Before starting the experiment

Since you don't have any proper NAND gate in LTSpice, you need to download NAND gate .rar file and extract NAND.sym and NAND.sch in your Experiment 6 folder, as given in Figure 1. Please save your experiment schematics to same folder that you created. During the experiment our voltage supply value is going to be 5V. It means that your logic 1 voltage value is 5V and your logic 0 voltage value is 0V.

PLEASE USE LABELS (RATHER THAN DIRECTLY CONNECTING THE SUPPLIES TO THE GATES), OTHERWISE IT WILL BE SO HARD TO SET THE CIRCUIT IN LTSPICE.

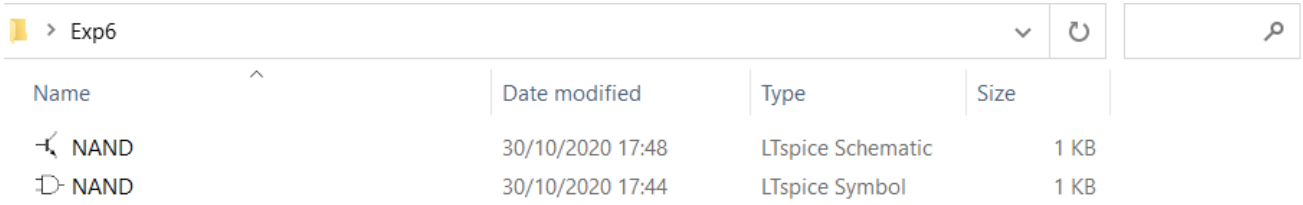

Figure-1: NAND .sch and NAND .sym files are in the same folder

Experiment 6.1.

In order to simulate the NAND gate please apply voltage waveforms below.

Input A: Vinitial: 0, Von: 5, Tdelay: 25m, Trise: 1m, Tfall: 1m, Ton: 23m, Tperiod: 50m
Input B: Vinitial: 0, Von: 5, Tdelay: 50m, Trise: 1m, Tfall: 1m, Ton: 48m, Tperiod: 100m

Outputs: Plot the voltages at nodes A, B, and OUT. Use add plot pane by clicking the mouse right button show your results. You are going to have 3 different plot pane.

Suggested Duration: 5 min.

Experiment 6.2.

NAND gate is a universal gate which means that you can obtain all the logic functions using only NAND gates. In this part, you will first get NOT operation, using one or several NAND gates and making connections properly. Then you will get AND operation and OR operation. Use De Morgan's Law to get OR operation. You can use the same input pulse waveforms in Experiment 6.1.

Outputs: Plot the input and output waveforms for NOT, AND and OR operations similar to the Experiment 6.1.

Show your results for each gates.

Suggested Duration: 15 min.

Experiment 6.3.

In Figure-2, you can see a cross-coupled inverter circuit. This circuit is an example of a bi-stable latch. Since you know how to use NAND gate as a NOT gate, you can set-up the circuit comfortably. In this configuration, you won't have any input. Do a 100 ms transient simulation and show your results at input of the each NOT gate. What is the problem for this circuit?

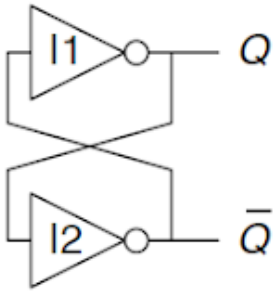

Figure 2: Cross coupled inverter.

Suggested Duration: 5 min.

Experiment 6.4.

In this part, you will investigate the operation of an SR-latch circuit. It is going to solve the problem in Experiment 6.3. Figure-3 shows NAND based SR-latch circuit. This circuit is an improved version of a cross-coupled circuit. Notice how similar two topologies are. SR-latch is a basic memory circuit. Simulate this circuit. You will use the same inputs in Experiment 6.1

Outputs: Plot the inputs and outputs.

Explain the operation of this circuit. Show your results. Do you still have any strange situation or disadvantage?

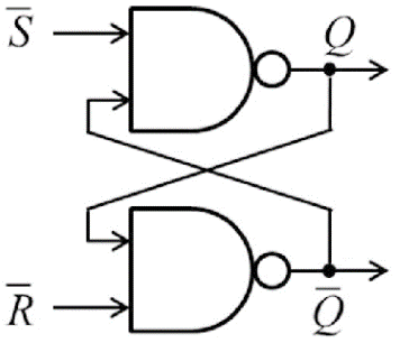

Figure 3: SR-latch

Suggested Duration: 10 min.

Experiment 6.5.

Figure-4 shows a D-latch circuit. This circuit is derived from SR-latch and it mitigates the problem in the SR-latch circuit. Make additions to your SR-latch and simulate the D-latch circuit. You are not allowed to use other than NAND gate when implementing this circuit (You must use NOT operation you derived in Experiment 6.2 using NAND gate).

Now, you will have a clock signal (CLK) and data signal (D) as given in Figure.4. Please apply D and CLK as given below. Only use Q signal as the output. (neglect Qbar)

Transient simulation must be done for 1s. (**.tran 1**)

Input D: Vinitial: 0, Von: 5, Tdelay: 22m, Trise: 1m, Tfall: 1m, Ton: 48m, Tperiod: 100m
Input CLK: Vinitial: 5, Von: 0, Tdelay: 50m, Trise: 1m, Tfall: 1m, Ton: 100m, Tperiod: 200m

Outputs: Plot the inputs (D, CLK) and outputs (Q).

Show your results and comment on the results.

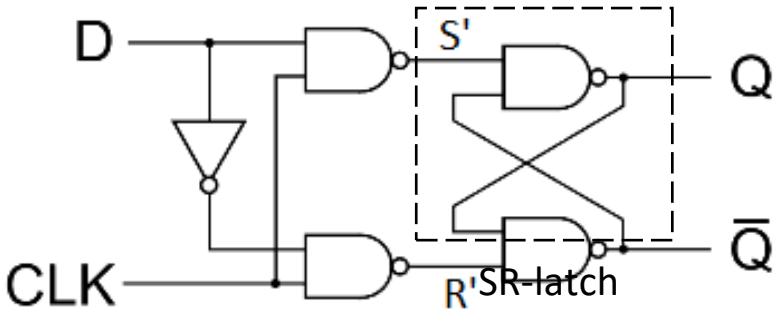

Figure 4: D-latch

Suggested Duration: 15 min.

Experiment 6.6.

Using two D-latches that you implemented in Figure.4, a D-flip flop can be obtained as shown in Figure-5. This circuit is a superior candidate for being a memory element. Duplicate your D-latch circuit and make appropriate connections to get D-flip flop. Only use Q signal as the output. (neglect Qbar) Please appy CLK and D signals as given below. You are going to use a PWL source for the data signal.

Input CLK: Vinitial: 0, Von: 5, Tdelay: 0, Trise: 1u, Tfall: 1u, Ton: 100m, Tperiod: 200m

Input Data: Insert PWL points exactly as given in below.

Time[s]	Value[V]
0	0
18m	0
18.1m	5
122m	5
122.1m	0
159m	0
159.1m	5
350m	5
350.1m	0
604m	0
604.1m	5
900m	5

Outputs: Plot CLK, D and Q and comment on the results.

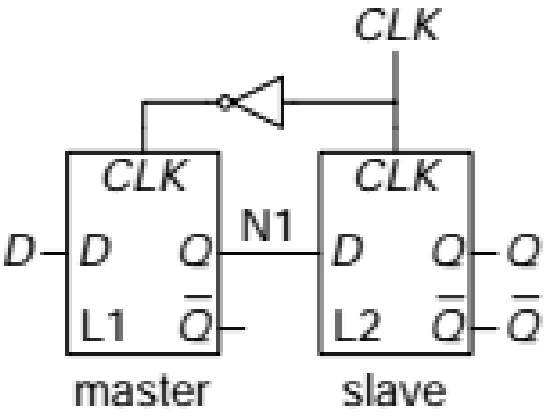

Figure 5: D-flip flop

Suggested Duration: 20 min.

Last Update: 31.10.2020