Experiment 3.1

NAND gate is a universal gate which means that you can obtain all the logic functions using only NAND gates. In this part, you will first get NOT operation, using one or several NAND gates and making connections properly. Then you will get AND operation and OR operation. Use De Morgan's Law to get OR operation.

Outputs: Derive the required circuitry for each logic gate.

Experiment 3.2

In this part, you will investigate the operation of an SR-latch circuit. Figure-1 shows NAND based SR-latch circuit. This circuit is an improved version of a cross-coupled circuit. Notice how similar two topologies are. SR-latch is a basic memory circuit.

Outputs: Derive the truth table.

Explain the operation of this circuit. Show your results.

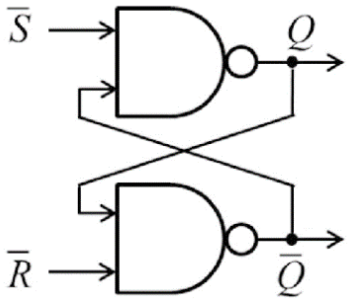

Figure 1: SR-latch

Experiment 3.3

Figure-2 shows a D-latch circuit. This circuit is derived from SR-latch and it mitigates the problem in the SR-latch circuit. Make additions to your SR-latch and arrive at the D-latch circuit. You are not allowed to use any gate other than NAND when implementing this circuit (You must use NOT operation you derived in Experiment 3.1 using NAND gate).

Outputs: Derive the truth table.

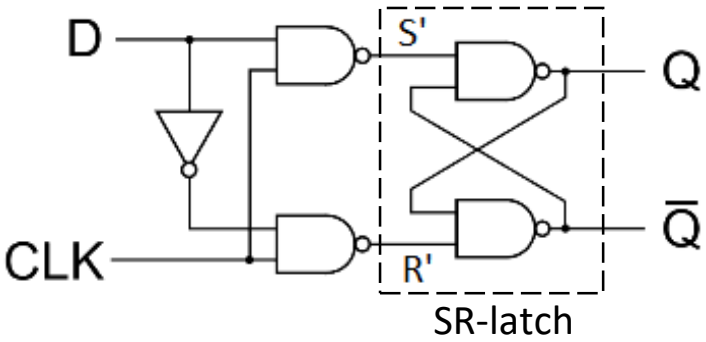

Figure 2: D-latch

Experiment 3.4

Using two D-latches that you implemented in Figure 2, a D-flip flop can be obtained as shown in Figure-3. This circuit is a superior candidate for being a memory element. Duplicate your D-latch circuit and make appropriate connections to get D-flip flop.

Outputs: Derive the truth table.

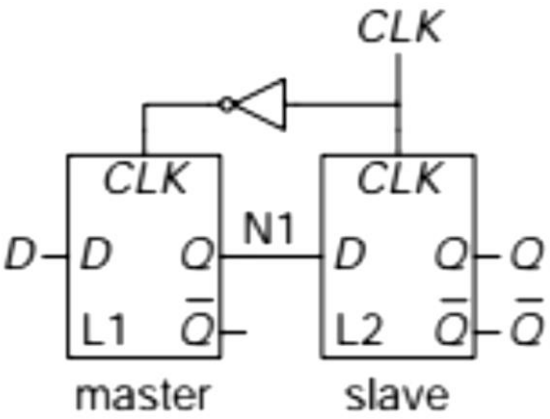

Figure 3: D-flip flop