ELE 312E
Analog Electronic Circuits Laboratory

Istanbul Technical University
Faculty of Elecrical and Electronics
Elektronics and Communication Department

Experiments

1- Low Frequency Power Amplifiers
2- Analog Integrated Circuit Building Blocks
3- Pulse and Frequency Response of BJT Amplifiers
4- Transistor Feedback Amplifiers
5- Characterization of PLL Building Blocks
6- Wide Band Amplifiers
7- Low Frequency Oscillators
8- Active Filters
9- PLL Applications
10- Switching Voltage Regulators

Analog Electronics Laboratory (ELE 312E)

Explanation about Laboratory

According to the "ITU Undergraduate Regulations of Faculty", grades of lessons for students are determined considering all students grades. Relative evaluation is done according to statistical distribution of grades and all students grades average. After relative evaluation, grades that specify success degree of students and expressed by letters are given to all students by instructors who give lectures.

Relative evaluation method produced by this system makes students effort to work hard with perfect performance during the laboratory works as much as in lessons.

- Students laboratory grades are determined according to the 10 laboratory works and the reports those must be done in term. Grade for one experiment is calculated with that rates: experiment work %70, experiment report %30. There is no final exam.
- Each of the students has 10 experiments and students have to do 9 experiments at least. Average grade is determined by dividing into 10 experiments for all situations.
- If students have valid excuse not to participate a laboratory experiment they have to give their medical report etc. (for medical issues) to laboratory coordinator or have to contact with laboratory coordinator for simultaneous examinations.
- Laboratory opens at 13:20 in days of the experiment. Students have to finish their experiments until 16:30.
- At least, one student in the group is responsible for handling the protocol paper to write test results during the experiment. Protocol paper can also be used as a scratch paper. After the experiment, each of the students in the group has to get a copy of the protocol paper. Students must deliver protocol paper (with same report cover) beside experiment report. Reports are only acceptable with protocol papers.
- Each of the students prepares only one report for each experiment. Student's name, surname, number, group number of experiment, date of experiment, experiment name and number, the research assistant's name and surname should be written by each student to the report cover completely. (An example of report cover is here www.elelab.itu.edu.tr)
- Reports are put to the report box near the entrance of the laboratory hall until one week after 12:30. Report box will be opened in experiment days before experiment hours by laboratory workers and reports will be given to the research assistants. After this time, the reports put to the report box will not be accepted. The report without protocol paper will not be accepted too. If report delivery day is holiday (public holiday or religious holiday etc.) the reports have to be put in the box until first working day 12:30.
- Experiment grades will be announced on the internet page within two days after report delivery.

Experiment works

The laboratory evaluation of the students is done according to the preliminary work, construction of the experiment and measurement evaluation of experimental results.

Preliminary work

Each of the students is tested before starting experiment by research assitant. This test may be written or oral examination. Those expectations are expected from students:

- Theoritical knowledge of the experiment that should be gotten from experimental sheet and other sources (lecture notes, books etc.). Experimental sheets can be bought from stationery at the beginning of the semester or can be downloaded from laboratory internet page. The theoritical information about experiment is not limited to study only experimental sheet, students have to research other sources to get enough knowledge.
- Students should know the purpose of the experiment. They should know how the experiment can be done and which measuring elements can be used. They should also get measuring elements catalog information.

Construction of the experiment

All of the students in each group should be participate in experiment. The following are considered to evaluate the experiment.

- Approach to the problem
- The accuracy of the results obtained
- The success of the questioning and interpreting the results (detect unrealistic results and have an idea about the causes)
- The use of tools (experiment material)
- The ability to deal with emerging challenges
- Efficient use of time
- The attention given to the experiment

Each of the students in group is evaluated separately for these matters.

The evaluation of the experimental results

After the experiments, the results are perused. The following should be considered:

- Interpretation of the experimental results (the meanings and results of the obtained data)
- Comparison of theoretical and experimental results.

Reports

Report is a technical writing which has experimental results and comments. The desired information should be clear, short and it should be undertaken easy. The prior knowledge and figures in experimental sheets should not be repeated in the report. They can be referanced.

Prepare a short report and do not forget to add protocol paper in the report.
The reports are evaluated according to format, technical content and results.

The following have to be in report:

- A brief introduction explaining the purpose of the experiment
- Presentation in charts about all of the measurement results (Students can use their protocol papers to get information and write results in charts.)
- Required graphs
- The theoritical calculations for comparison (Results are in charts.)
- Comments on each measurement
- The conclusion part which is short and includes comments of results and general evaluations

The reports can be writed on computer or by hand with using only black or blue pen without using pencil (except for graphs). All attachments (graphs, protocol paper) should be attached to the report tightly.

If you encounter such a problem the laboratory coordinator will be eligible to apply.

Analog Electronics and Introduction to Electronics Laboratory Scoring Test Reports

Main Title	Subheading	Score
Report Layout	The preparation of the report cover (Name, Number, Department, Test Date, Experiment Title, Group Number)	**10**
	The general structure of the report (Proper use of Turkish, page structure, shape, and graphic layouts, page number, etc.)	
Information about the Experiment and Experimental Procedure	The purpose of the experiment, brief information about the experiment, what is done in the experiment	**20**
Theoretical Calculations	Calculations and (if there are) simulations (Pspice ect.)	**30**
Evaluation, Comparison and Interpretation of Simulation Results, Measurements and Calculations	Preparing a table to compare the data, determination of differences, to review, evaluate skills gained in the experiment	**40**
	Preparation of graphs clearly (Output color, the presence of the desired measurements, logical and proper selection of axes, named graphics, etc.)	
	TOTAL	**100**

Issues must be considered:

- Reports do not include technical calculations,
- Reports are prepared with pencil,
- Copy reports,

ARE INVALID!!!

Last Update: 28.02.2013
The contributors to prepare sheet:
Bülent Yağcı (General Coordinator), Mehmet Duman (Introduction and Layout of Sheet), Zafer İşcan (Experiment 1), Nazan İltüzer (Experiment 1), P. Başak Başyurt (Experiment 3), Osman Ceylan (Experiment 4), Ayan Derya (Experiment 5 ve 9), Berat Doğan (Experiment 6), Vedat Tavas (Experiment 6), Hacer Yıldız (Experiment 7), Sinem Keleş (Experiment 8), Gürer Özbek (Experiment 10)

EXPERIMENT 1

Low Frequency Power Amplifiers

Purpose

Class B/AB power amplifiers operation should be understand and these amplifiers should be compared about efficiency and distortion.

Preparation for Lab 1

- **Subjects needed to look at before coming to lab**
  - Class A/B/AB Power Amplifiers
  - Distortion
- **Calculations**
  - Calculate R_1 and R_2 in Figure 8 with assuming the circuit operates at Class B condition and the output voltage swing is symmetrical (the output is biased at 7.5V). (Transistor parameters are β_F=250 and V_{BE}=0.6V).
- **Pspice Simulation**
  - Design the circuit with using Spice model parameters and find the appropriate R_1 and R_2 values for the Class B operation. (The bias point of output should be 7.5V.)
  - When a sinusoidal input signal is applied with maximum swing and 1 kHz frequency for Class B operation and R_L=10Ω, plot the symmetrical output voltage. Calculate output power and efficiency.
  - When a sinusoidal input signal is applied with maximum swing and 1 kHz frequency for Class AB operation (Class AB operation can be provided with choosing appropriate R_2 value) and R_L=10Ω, plot the symmetrical output voltage. Calculate output power and efficiency.

Model parameters of BD135:

.MODEL BD135 NPN (IS=4.815E-14, NF=0.9897, ISE=1.389E-14, NE=1.6, BF=124.2, IKF=1.6, VAF=222, NR=0.9895, ISC=1.295E-13, NC=1.183, BR=13.26, IKR=0.29, VAR=81.4, RB=0.5, IRB=1E-06, RBM=0.5, RE=0.165, RC=0.096, XTB=0, EG=1.11, XTI=3, CJE=1.243E-10, VJE=0.7313, MJE=0.3476, TF=6.478E-10, XTF=29, VTF=2.648, ITF=3.35, PTF=0, CJC =3.04E-11, VJC =0.5642, MJC=0.4371, XCJC=0.15, TR=1E-32, CJS=0, VJS=0.75, MJS=0.333, FC=0.9359)

Model parameters of BD136:

.MODEL BD136 PNP (IS=7.401E-14, NF=0.9938, ISE=4.104E-16, NE=1.054, BF=336.5, IKF=0.1689, VAF=22.47, NR=0.9913, ISC=1.290E-14, NC=1.100, BR=13.91, IKR=9.888E-2, VAR=30, RB=0.5, IRB=1E-06, RBM=0.5, RE=0.208, RC=5.526E-02, XTB=0, EG=1.11, XTI=3, CJE=1.066E-10, VJE=0.69, MJE=0.3676, TF=2.578E-10, XTF=13.56, VTF=2.366, ITF=1.304, PTF=0, CJC=5.234E-11, VJC=0.6431, MJC=0.4436, XCJC=0.44, TR=1E-25, CJS=0, VJS=0.75, MJS=0.333, FC=0.99)

Model parameters of BC237:

.MODEL BC237 NPN (IS=1.8E-14, ISE=5.0E-14, NF=0.9955, NE=1.46, BF=400, BR=35.5, IKF=0.14, IKR=0.03, ISC=1.72E-13, NC=1.27, NR=1.005, RB=0.56, RE=0.6, RC=0.25, VAF=80, VAR=12.5, CJE=13E-12, TF=0.64E-9, CJC=4E-12, TR=50.72E-9, VJC=0.54, MJC=0.33)

Introduction

Generally, the analog circuits have an input and output stage. The output stage should deliver the output signal to the load without loss of gain. The output stage is the final stage of the

amplifier and the signal is large in that stage. Therefore, the small signal approximations and models are not appropriate to use. However, the linearity still is an important parameter.

The required amount of power should be delivered to the load efficiently. The power dissipated in the output stage transistor must be as low as possible.

In the literature, there are various output stage configurations in amplifiers.

If the input signal is delivered to the load without distortion, then the equation (1) can be used.

$$V_o = KV_i \quad (1)$$

V_o:The amplitude of the output signal, V_i: The amplitude of the input signal, K: constant

The circuit can be accepted as linear from the equation (1) but the large signal characteristics of the active components in electronic circuits are known as nonlinear. Therefore, the distortion is observed in the output signal.

If an sinusoidal input signal is applied to an amplifier and the input-output characteristic is given as $V_o = f(V_i)$ from Figure 1,

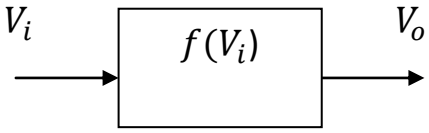


Figure 1: Input-output characteristic of an amplifier.

From Figure 1, the equation (2) can be given with using Taylor series.

$$V_o = A_o + A_1V_i + A_2{V_i}^2 + A_3{V_i}^3 + \cdots \quad (2)$$

If V_i equals to $sinwt$, the equation (3) can be written with using trigonometric calculations.

$$V_o = B_o + B_1 sinwt + B_2 sin2wt + B_3 sin3wt \quad (3)$$

The harmonics of the output signal can be seen from equation (3) because of the nonlinear characteristic of the amplifier. The output power in the fundamental frequency is the frequency of the input signal is given in equation (4).

$$P_1 = \frac{{B_1}^2}{2R_L}, \qquad R_L\text{: Load resistance} \quad (4)$$

The total power which is delivered to load (P) (equation 5):

$$P = \frac{1}{2R_L}({B_1}^2 + {B_2}^2 + {B_3}^2 + \cdots) \quad (5)$$

The relation between the output power in the fundamental frequency and the total power is given in the equation (6).

$$P = (1 + D^2)P_1 \quad (6)$$

$$D_i = \frac{B_i}{B_1}, \qquad D = \sqrt{{D_2}^2 + {D_3}^2 + {D_4}^2 + \cdots}$$

D shows the total harmonic distortion and it represents how much the input signal is distorted. Distortionmeter is used to measure the distortion in the circuit. In distortionmeter, a notch filter is used to eliminate the signal in the fundamental frequency as shown in Figure 2, then the power of the harmonics are summed.

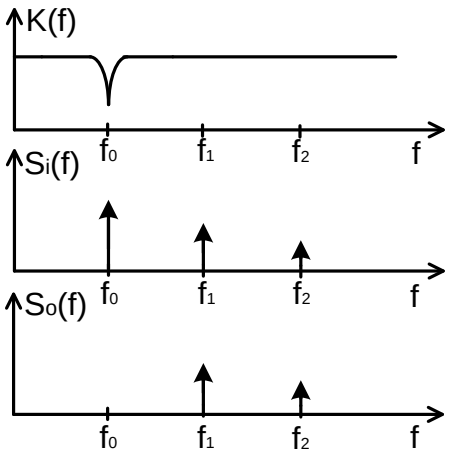


Figure 2. Eliminating the fundamental frequency with notch filter.

In Figure 2, K(f)-f shows the gain-frequency characteristic of the notch filter, $S_i(f)$-f shows the harmonics (f_1, f_2) and the fundamental frequency (f_0) of the signal and $S_o(f)$-f shows the output of the notch filter.

Power amplifiers (A, B, AB, C, D, E, F, G, H) are classified as their biasing point conditions.

In this experiment, only class B and AB would be observed. The output stages of these amplifiers are generally complementary pair of transistors.

Class B Operation: In class B operation, the transistors at the output stage cannot conduct simultaneously.

When the input voltage is zero, both transistors are cut off.

When the input signal is positive and exceeds V_{BE} then T_1 conducts and T_2 is cut off. T_1 supplies the load current.

When the input signal is negative and exceeds $-V_{BE}$ then T_2 conducts and T_1 is cut off. T_2 supplies the load current.

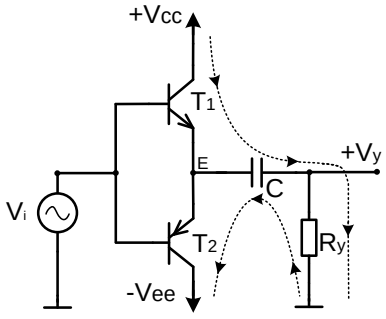


Figure 3: Class B amplifier configuration with two supply voltages.

The disadvantage of this operation is the crossover distortion in the output signal. It occurs when both transistors are in cut off region.

The base emitter voltage (V_{BE}) and collector current (I_c) characteristic of a bipolar npn transistor is given in Figure 4. When the current is zero (until V_γ), characteristic has a large amount of nonlinearity.

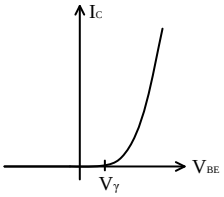


Figure 4. Base emitter voltage and collector current characteristic of a bipolar npn transistor.

In Figure 5, I_c- V_{BE} characteristics of class B output stage transistors and crossover distortion is shown. When I_{c1} and I_{c2} are zero, the crossover distortion is observed.

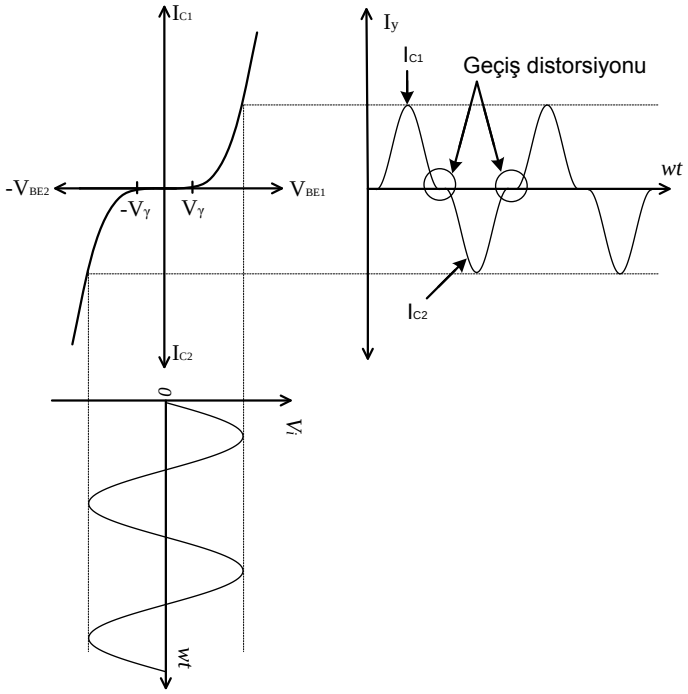


Figure 5. I_c- V_{BE} characteristics of class B output stage transistors and crossover distortion.

Class AB operation: In order to cancel the crossover distortion, complementary transistors are biased at a different biasing point and even when there is no input signal, there is a low amount of current in T_1 or T_2. In Figure 6, class AB output stage with driver stage is shown.

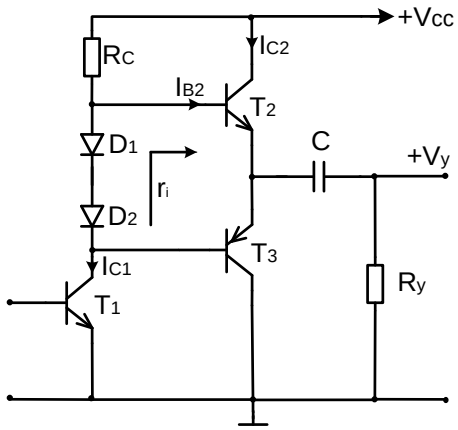
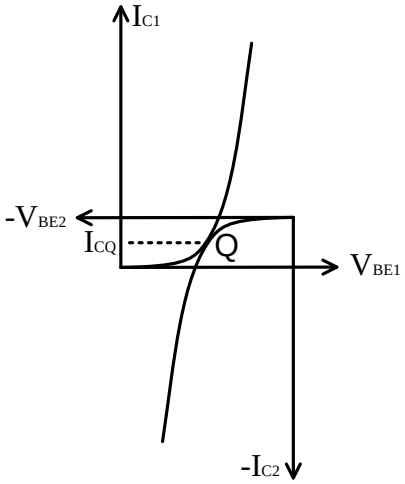


Figure 6: Class AB output stage with driver stage.

In Figure 6, D_1 and D_2 diodes supplies V_{BE} voltages for complementary transistors.



Şekil 7: I_c- V_{BE} characteristics of class AB output stage transistors and the biasing point (Q).

I_c- V_{BE} characteristics of class AB output stage transistors and the biasing point (Q)

are given in Figure 7. At biasing point, there is a low amount of current (I_{CQ}). Therefore, the crossover distortion is not observed, but because of this current, the efficiency is decreased.

References:

1) D. Leblebici, Elektronik Devreleri, İTÜ Matbaası, 1992.
2) A. B. Grebene, Bipolar and MOS Analog Integrated Circuit Design, Wiley Classics Library, 2001.
3) P. R. Gray and R. G. Meyer, Analysis and design of analog integrated circuits, John Wiley, 1993.
4) M. S. Türköz, Elektronik, Birsen Yayınevi, İstanbul, 2004.

Experiment:

The circuit in Figure 8 should be setted up with applying a 1 kHz sinusoidal input voltage (V_G).

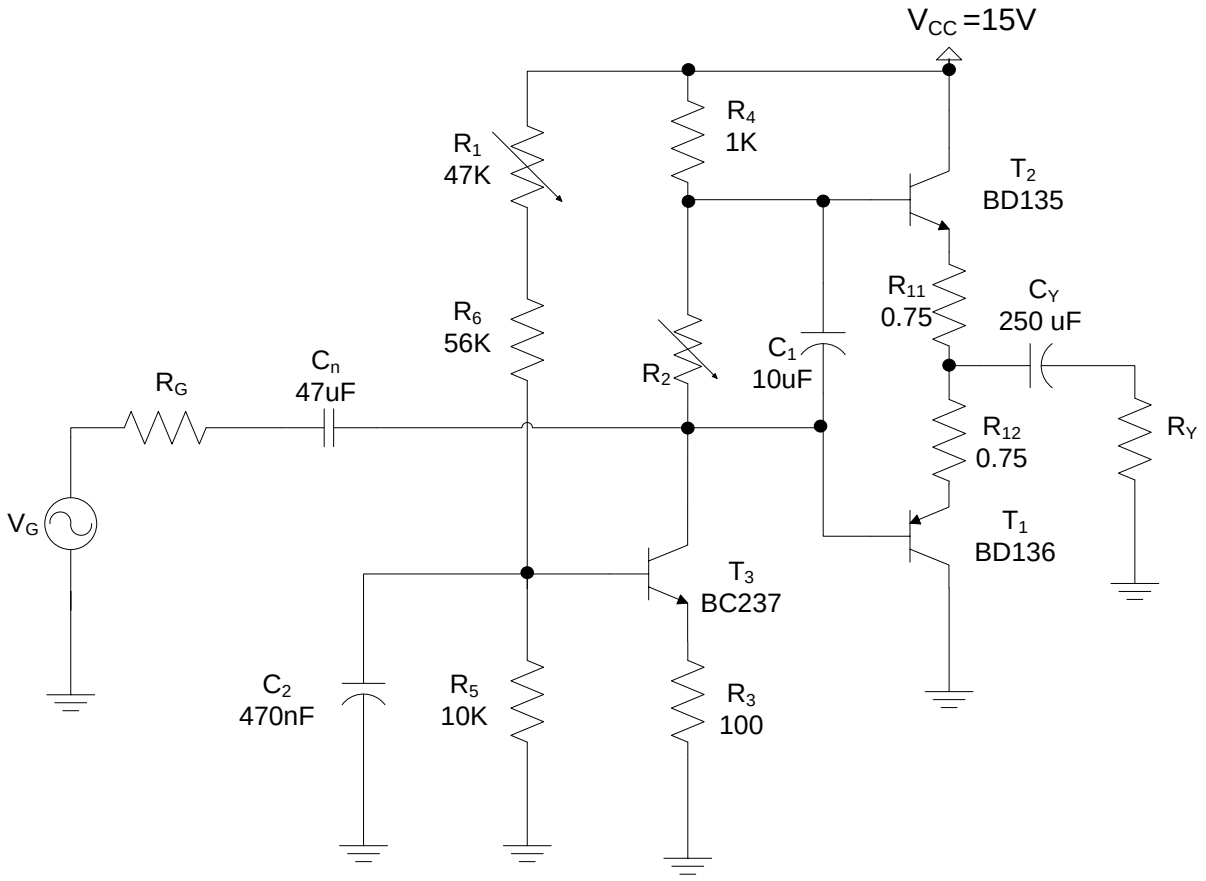


Figure 8. Class B and AB power amplifier circuit.

1. (a) With changing the value of the resistance R_2, provide the circuit to be worked as class B. (The crossover distortion is seen in Class B operation.). In order to provide the maximum output voltage, resistance R_1 should be changed. The output signal should be plotted.

(b) For different amplitude values of the output signal in class B operation, Table 1 should be done.

2. (a) With changing the value of the resistance R_2, provide the circuit to be worked as class AB. (Be careful to not to increase the current consumption in the circuit, the crossover distortion should not be seen as it was in Class B operation.). The output signal should be plotted.

(b) For different amplitude values of the output signal in class AB operation, Table 2 should be done.

3. In class AB operation, square wave signal should be applied. Then the Table 3 should be done for a chosen amplitude value in Table 2.

Lab #1
LOW FREQUENCY POWER AMPLIFIERS

Experiment date:	
Name of assistant:	
Signature:	

Grup	**Student Number**	**Name and surname of the student**

Table 1: In Class B operation (Sinusoidal wave) - $P_y = {V_o}^2/2R_y$, $P_{DC} = V_{CC}I_{CC}$, $\eta = P_y/P_{DC}$

The values of output voltage (Vo), Distortion (D), Supply current (Icc) and efficiency (η)							
Load resistance: **R_Y=10Ω**					Load resistance: **R_Y=40Ω**		
V_0(V)	**D(%)**	**I_{CC}(mA)**	**Verim(η)**	**V_0(V)**	**D(%)**	**I_{CC}(mA)**	**Verim(η)**
0.5				**0.5**			
1				**1**			
1.5				**1.5**			
2				**2**			
2.5				**2.5**			
3				**3**			
3.5				**3.5**			
4				**4**			
4.5				**4.5**			
5				**5**			
5.5				**5.5**			
6				**6**			

Tablo 2: In Class AB operation (Sinusoidal wave)- $P_y = {V_o}^2/2R_y$, $P_{DC} = V_{CC}I_{CC}$, $\eta = P_y/P_{DC}$

The values of output voltage (Vo), Distortion (D), Supply current (Icc) and efficiency (η)							
Load resistance**: R_Y=10Ω**					Load resistance**: R_Y=40Ω**		
V_0(V)	**D(%)**	**I_{CC}(mA)**	**Verim(η)**	**V_0(V)**	**D(%)**	**I_{CC}(mA)**	**Verim(η)**
0.5				**0.5**			
1				**1**			
1.5				**1.5**			
2				**2**			
2.5				**2.5**			
3				**3**			
3.5				**3.5**			
4				**4**			
4.5				**4.5**			
5				**5**			
5.5				**5.5**			
6				**6**			

Tablo 3: Class AB operation (Square wave) - $P_y = {V_o}^2/R_y$, $P_{DC} = V_{CC}I_{CC}$, $\eta = P_y/P_{DC}$

Yük Direnci: **R_Y=40Ω**			
V_0(V)	**D(%)**	**I_{CC}(mA)**	**Verim(η)**

EXPERIMENT 2

Analog Building Integrated Circuits Blocks

Introduction and Objective

With the rapid improvement of integrated circuits technology in the electronics fields, integrated circuits have been replace the discrete circuits elements. It is provide us that easy to use this integration which have a lot of benefits. Some of these advantages production identical elements, small size with high performance and reliability. The first half of the eighties , bipolar and MOS technology are used analog and digital circuit design, respectively. At nineties, MOS technology also used to conduct analog process.

In this study , some of these basic building blocks used in analog integrated will examine.

Foreknowledge

Transistor current sources are use both polarization and amplification as a load elements especially in analog integrated circuits. In the cases of using polarization , it decreases dependences of circuits to temperature and power supply. Because of the less size agains to resistance in analog circuits is preferred especially low currents. Thanks to the greater output resistance, larger output can be achieved when it uses as a active load element. The simplest current source can be achieved as following Figure 1.

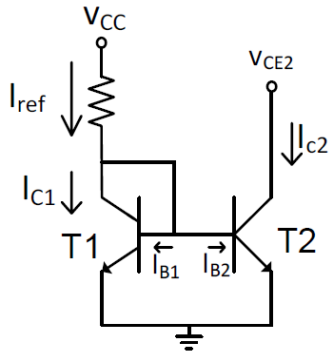


Figure 1.Simple current source (Current mirror)

The output resistance of T2 is infinite (I_{c2} is independent from V_{cE2}) , in the case of T1 and T2 are identical transistor, Equation 1 and Equation 2 are obtained as following.

$$I_{C1} = I_{C2} \qquad (1)$$

$$I_{C2} = \frac{Iref}{1+\frac{2}{hFE}} \qquad (2)$$

In reality, output resistance is not infinite . I_{c2} is not stable as collector voltage changes (Figure 2). It means that collector current is increased by increasing collector voltage.

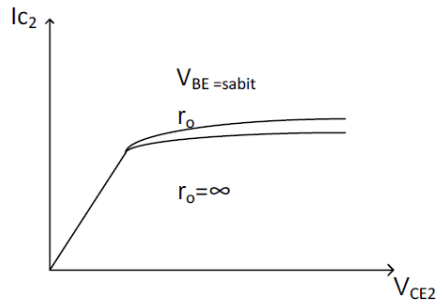


Figure 2. Collector charecteristics in the case of r0 =∞ and r0 has a finite value for npn transistor.

Effect of the base-width modulation (Early Effect) is described as following.

$$Ic = Is\, e^{VBE/VT}\ (1 + \frac{V_{CE2}}{VA}) \qquad (3)$$

Here, V_A show early voltage. When it comes to larger supply power , output resistance remain small (dependence of V_{CE2} become higher). Ratio of I_{ref} /Ic2 is may be quite different than in the case of ignoring of effect of output resistance.

To examine the simple current source , set up circuit in Figure 3. For I_{ref} less than 5 mA figure out the charecteristic of $I_{ref} - I_{C2}$. Using this measurement, calculate approximate value of V_A and h_{FE} .

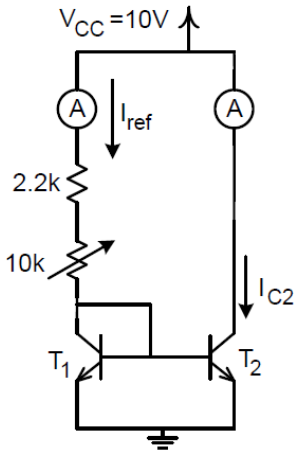


Figure 3.

Replaced circuits in Figure 3 into Figure 4 and with the absence of P_2 potentiometer, using P_1 potentiometer regulate referans current to $I_{ref} \approx 2$ mA. In this situation , measure I_{c2} current and V_B voltage. Fix the the $I_{ref} \approx 2$ mA and change the V_{c2} voltage between 1V-10 V with using P_2 potentiometer. When the one of measured values is $V_{CE2} = V_{CE1}$, figure out characteristic of I_{c2}-V_{CE2} and compare the estimated value .

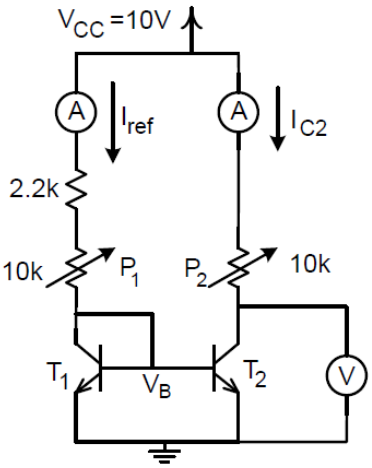


Figure 4.

Using the referance current (I_{ref}), it is estimated that current source which more than one is produced in most application.(Figure 5)

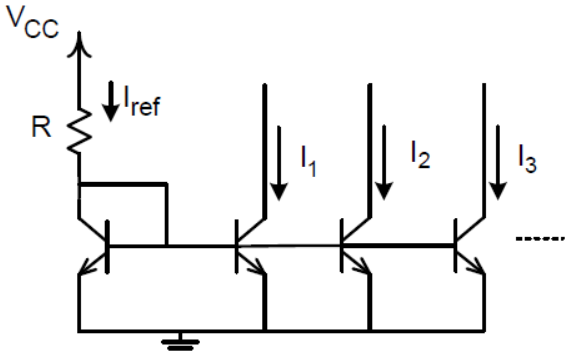


Figure 5. Simple current source with multiple output.

In this case , how the current moving each branch changes depending on the I_{ref} and output number?

To increase the output resistance , circuit in Figure 6 may be recommended. In this case , obtain connection between I_{c2} and I_{ref} by using circuit in Figure 6. For simple current source that have emitter resistance, consider R_1= R $_2$=1 KΩ and obtain characteristics of I_{C2} –I_{ref} , I_{C2}-I_{CE2} with using the circuits in Figure 6 and Figure 6b, respectively. Compare and comment the results with former circuits outcome .

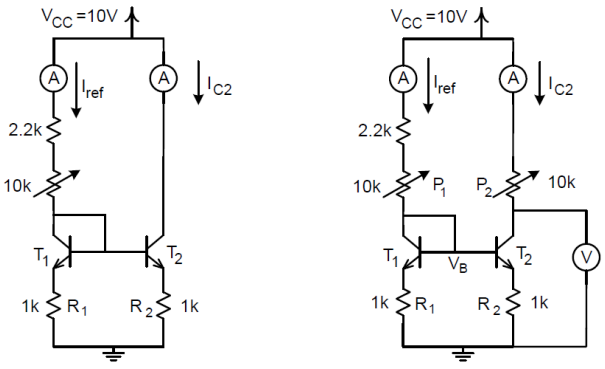


Figure 6.Simple current source with emitter resistance

Think about the design of way to change the ratio of I_{C2}/I_{ref} when you want. Wilson current source generally uses get rid of disadvantages of simple current source. Calculate the ratio of I_{c2}/I_{ref} of Wilson current source given by Figure 7a. With helping of Figure 7 b, examine the theoretical changes of I_c with V_c. Calculate the output resistance of circuits.

Same as the former calculation, for same interval and measurement methods figure out characteristics of I_{C2}-I_{ref} and $I_{c2} - V_{CE2}$ by using the Figure 7a. Compare and comment the result with former results.

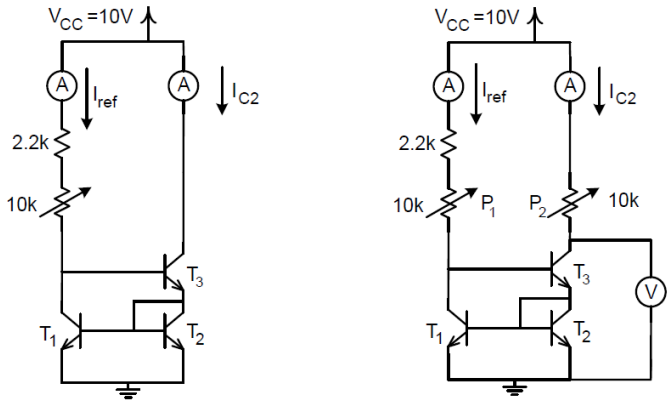
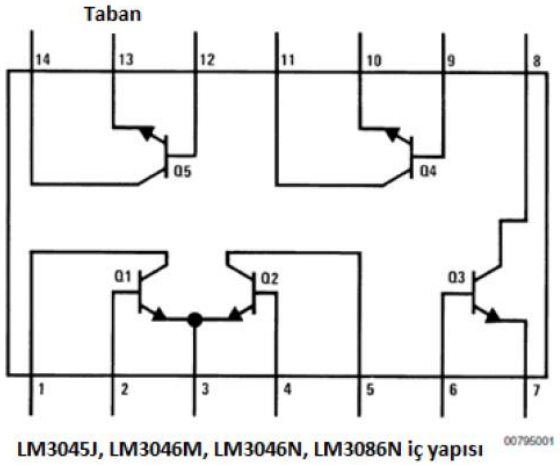


Figure 7.Wilson current source

Note:3046(3086) integrated circuits transistor series will be used in experiments.



References

- Analog Elektronik Devreleri, Duran Leblebici,İTÜ matbaası, İstanbul, 2001.
- Analog Tümdevre Tasarımı, Hakan Kuntman, Sistem Yayıncılık, İstanbul, 1992.
- Elektronik Devreleri, Sait Türköz, Birsen Basıs Yayın, İstanbul,1999.

EXPERIMENT 3

Pulse and Frequency Response of BJT Amplifiers

Preliminary work

Useful topics

- What is an amplifier? Which parameters affect the performance of an amplifier?
- What are the main features of single-transistor amplifier stages?
- What are the important frequency values of gain-frequency curve of an amplifier? How are they obtained?
- What are rise time and pulse droop? Which parameters affect the values of rise time and pulse droop?

Theoretical calculations

- Derive the equations necessary for the calculation of quiescent (Q) point voltage and current values of the circuit in Figure-4. Calculate the values of R_1, R_2, R_C and R_E resistors so that it satisfies the specifications given below:
  - peak to peak unclipped 10V voltage difference should be obtained across the load (R_Y=15 kΩ)
  - Value of collector current of Q point: I_{CQ}=0.95 mA,
  - Minimum value of small signal equivalent input resistance: R_i= 5 kΩ
- Calculate the small signal gain of the amplifier.
- Calculate the values of capacitors in the circuit so that pole frequency caused by the effect of each capacitor will be 200 Hz. Calculate the lower cut-off frequency.
- Calculate the values of the capacitors in the circuit so that pulse droop will be %5 caused by the effect of each capacitor. Assume you applied a pulse wave to the input whose pulse-width is 10 μs.

(R_g = 600Ω, Trans. Par.: V_{CEsat} = 0.2V, h_{FE} = 230, h_{fe} = 330, h_{oe} = 20μA/V, f_T = 120MHz, $C_{cb'}$ = 2.5pF)

Circuit analysis using Pspice

- Obtain the DC quiescent point of the circuit (I_{CQ}, V_{BQ}, V_{CQ} and V_{EQ}) using the resistor values calculated in preliminary work.
- Sketch the freguency-gain curve of the circuit and determine the cut-off frequencies using the capacitor values calculated in preliminary work.
- Observe the pulse-response of the circuit (pulse droop and rise time) using the capacitor values calculates in preliminary work. (Choose proper values for amplitude and frequency of the input signal)

P.S: "Useful topics" is not required as written. Related topics should be researched/ studied in order to understand the experiment better. Theoretical calculations and printed PSpice simulations will be collected and scored as "preliminary report". In addition, written/oral exam performed during/before the experiment, will be graded as a part of "experiment score".

Objectives:

Amplifiers are the circuits which amplifies the input signal supplied by a signal generator and transfers it to the load. Depending on the aim, they are designed to transfer voltage, current or power to the load. Using amplifier circuits, time-varying output signals are generated by superimposing time-varying input signals and DC components.

In this experiment, change of a time-dependent signal at the output of an amplifier will be examined.

Introduction:

The gain is defined as the ratio of guantity measured at the output to quantity measured at the input. There are three types of gain which are: voltage gain, current gain and power gain. The gain, input empedance and output empedance are important to determine the behaviour of a circuit. A two-port amplifier is presented in Figure-3.1.

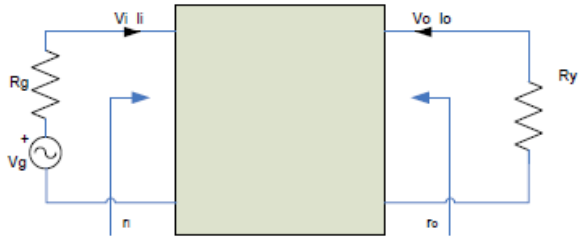


Figure 3.1 2 port amplifier

The highest gain of an amplifier can be obtained in the absence of signal-loss at the input and output of the amplifier. This condition is satisfied for a voltage amplifier in the case of input resistance is infinite and the output resistance is zero.

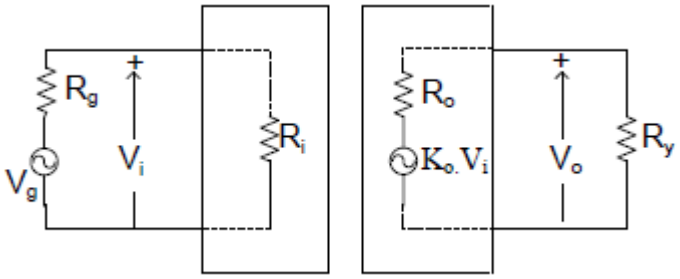


Figure 3.2 Equivalent circuits of input and output stages of the amplifier

For the block diagram of an amplifier in Figure-3.2, the input resistance is represented by R_i, the output resistance is R_o and the open-loop gain is K_o.

The relation between input voltage (V_i) and source voltage (V_g) is:

$$V_i = V_g \frac{R_i}{R_i + R_g}$$

As seen, to obtain V_i=V_g , the condition $R_i \gg R_g$ should be satisfied. Similarly, the relation between output voltage of the amplifier without load ($K_o.V_i$) and output voltage (V_o) can be written as:

$$V_o = K_o V_i \frac{R_y}{R_o + R_y}$$

From the equation, it can be seen that maximum value of output voltage is V_o=$K_o.V_i$. This value is reached if the condition $R_o \ll R_y$ is satifsied.

The curve plotted for the change in gain of the amplifier versus frecuency is called gain-frequency curve (Figure-3.3).

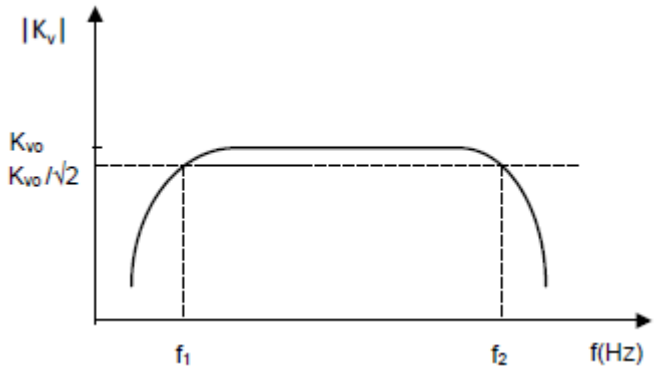


Figure 3.3 Gain-frequency curve of an amplifier

If high gain is desired, multiple stages of single-transistor circuits are connected in cascade form. In this case, the previous stage's DC conditions shouldn't affect the next stage's operating conditions. In addition, the signal source connected to the input and the load connected to the output shouldn't change the operating conditions of the amplifier. Therefore, coupling capacitors can be used to insulate the circuit from DC components for low-frequency applications.

For the components needed for DC signals but not necessary for AC signals, by-pass capacitors can be used. Both of coupling and by-pass capacitors affect the frequency response of the circuit.

Common-emitter amplifier:

In these circuits, base is the input terminal, collector is the output terminal and emitter is common for input and output. Since the input resistance of the common-emitter amplifier is higher than the common-base amplifier's, it is more suitable to be used for cascade connection.

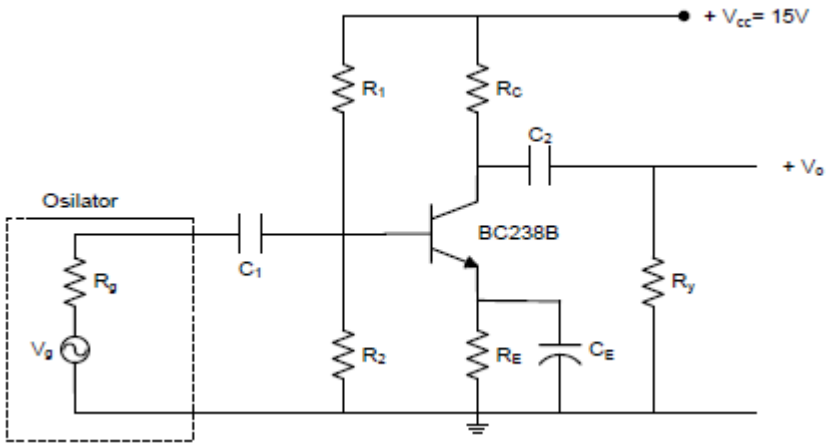


Figure 3.4 Common-emitter amplifier

By DC analysis, assuming $I_B << I_C$, the equations below can be written:

$$V_{CC} = V_{CEQ} + I_{CQ}(R_E + R_C) \quad (1.1)$$

$$R_{DC} = R_E + R_C \quad (1.2)$$

$$R_{AC} = \frac{R_C R_Y}{R_C + R_Y} \quad (1.3)$$

If the line corresponds to Equation 1.1 is plotted (DC load line) , I_B will be the intersection point of this line and characteristic curves of the amplifier. DC load line intersects the horizontal axis at the V_{CC}/R_{DC} point and its slope is $-1/R_{DC}$. The other line, which is called AC load line, intersects the characteristic curves at the same point (I_B) and its slope is $-1/R_{AC}$. Since R_{AC} is not equal to R_{DC} , their intersection points with the axes will be different. (Figure-3.5)

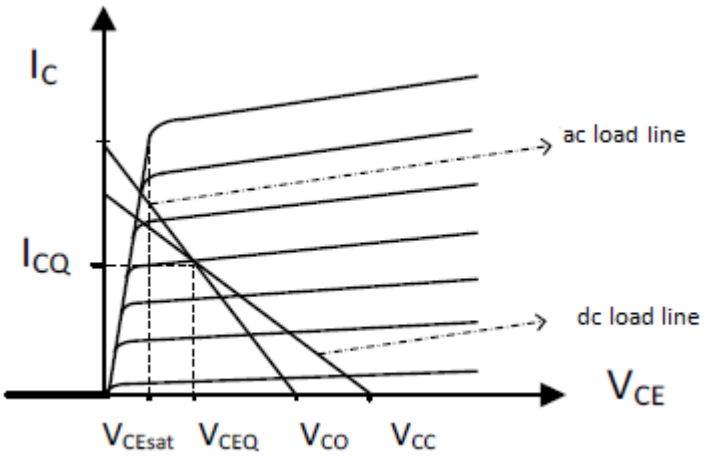


Figure 3.5 Characteristic curves of an amplifier

Using slope of AC load line, equation for V_{CO} can be derived (Equation-1.4). If Equation-1.1 is substituted in Equation-1.4, we get Equation-1.5.

$$V_{CO} = V_{CEQ} + R_{AC}.I_{CQ} \tag{1.4}$$

$$V_{CO} = V_{CC} - (R_{DC} - R_{AC}).I_{CQ} \tag{1.5}$$

If a time-varying signal is applied as input to the circuit, the value of collector current will change hence the voltage difference between collector-emitter will also change. The amount of variation is limited by V_{CEsat} and V_{CO} as seen in equations below:

$$V_p = V_{CO} - V_{CEQ} = R_{AC}.I_{CQ} \qquad V_n = V_{CEQ} - V_{CEsat} \tag{1.6}$$

As a result of proper choice of the values for quiescent point, the amount of clipping for positive and negative alternance will be equal, so the symmetric clipping condition can be written as below:

$$V_{CEQ} - V_{CEsat} = V_{CO} - V_{CEQ} = R_{AC}.I_{CQ} \tag{1.7}$$

$$I_{CQ} = \frac{V_{CC} - V_{CEsat}}{R_{DC} + R_{AC}} \tag{1.8}$$

Amplifying the input signal without distorting its shape is called as linear amplfication. In other words, the output of a linear amplifier is always proportional to its input. Since this condition cannot always be satisfied, output signal will differ from the input signal although the circuit is linear. The causes of these distortions are the internal parasitic capacitances of the circuit, the coupling capacitors and the by-pass capacitors. High valued capacitors cause distortion for the signals in low frequency range, but low valued capacitors and parasitic capacitances affect the circuit in high frequency range.

Pulse response:

Ideally, if a square wave is applied as input to an amplifier, a square-wave is expected at the output. But, because of the parallel capacities seen in equivalent circuit of the amplifier, the output signal

cannot change at the same time with the input signal. Since the coupling and by-pass capacitors are considered as short-circuit for quick-changes of the signal, the equivalent circuit shown in Figure-3.6(a) can be used to analyze the behaviour of the circuit for such signals.

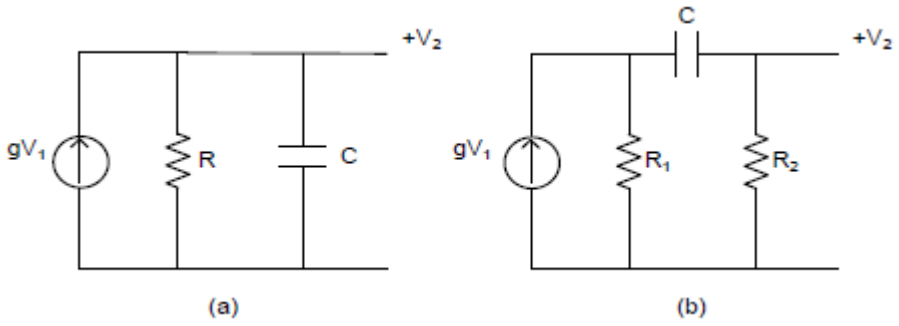


Figure 3.6 Equivalent circuits of an amplifier

a) High-frequency b)Low-frequency

If a pulse wave is applied to the input of the circuit given in Figure-3.6(a), the equation for the output can be written as:

$$V_2(t) = K_o.V.(1 - e^{-t/\tau})$$

Here, τ is time-constant, V is the amplitude of pulse-signal and K_o is voltage gain of the amplifier. The time required for the response to rise from 10% to 90% of maximum value of $V_2(t)$ is called as rise time (t_r). Rise time of the output can be calculated using the equation below.

$$t_{r=}2{,}2.\tau = 2{,}2.R.C$$

For the circuits in cascade form, rise time can be calculated using rise time of each stage as given in the equation below:

$$t_r \cong 1{,}1.\sqrt{t_{r1}^2 + t_{r2}^2 + \cdots + t_{rn}^2}$$

As a result, the output signal of an amplifier whose input signal is a pulse-signal, rises during rise time and reaches to a value higher than its value at rest. If a capacitor is used for coupling in this circuit, the output signal can't keep its new value and decreases until it reaches to the value at rest. This behaviour can be analyzed using the circuit given in Figure-3.6(b).

If a pulse wave is applied to the input of the circuit given in Figure-3.6(b), the equation for the output can be written as:

$$V_2(t) = K_o.V.(e^{-t/\tau})$$

Here, V is the amplitude of pulse-signal , K_o is voltage gain of the amplifier and τ is time-constant:

$$\tau = (R_1 + R_2).C$$

The change of the signal corresponds to this equation is shown in Figure-3.7(b). As it can be proven from the equation, at the time t= τ, amplitude of the output signal is 1/e of its value at the begining. This decrement is called as pulse droop and it can be calculated using the equation given below:

$$F = \frac{T_D}{\tau}$$

Not only coupling capacitors, but also by-pass capacitors cause pulse droop and its value can be calculated using equation below:

$$F = \frac{T_D}{C_E r_e}$$

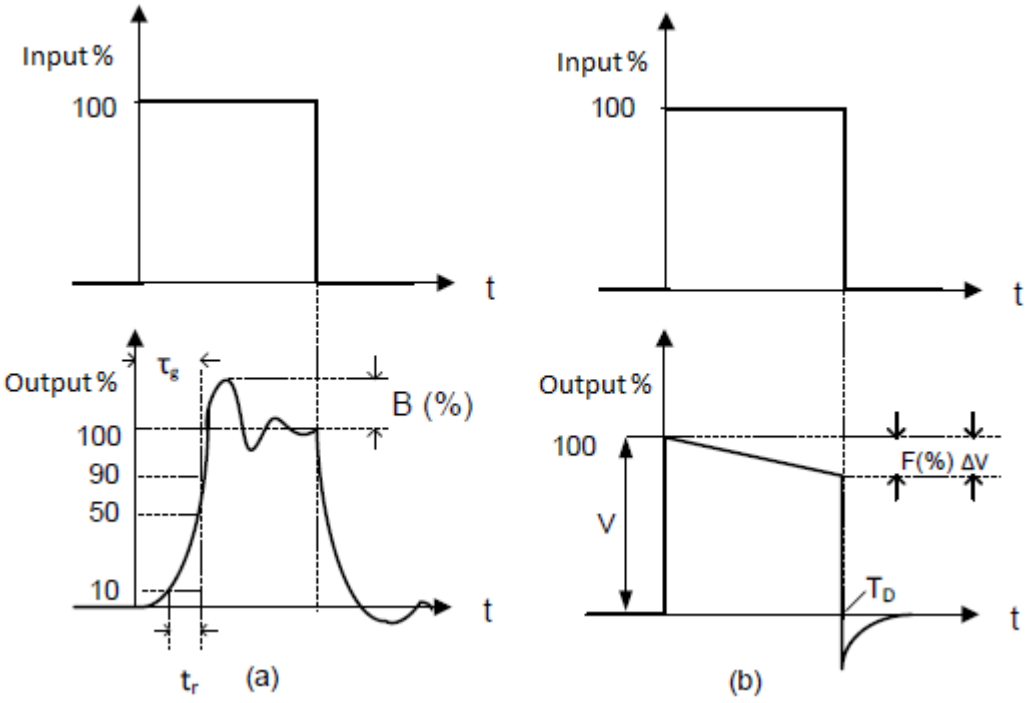


Figure 3.7 a) Response of an amplifier to a high-frequency pulse
b)Response of an amplifier to a low-frequency pulse

Kaynaklar

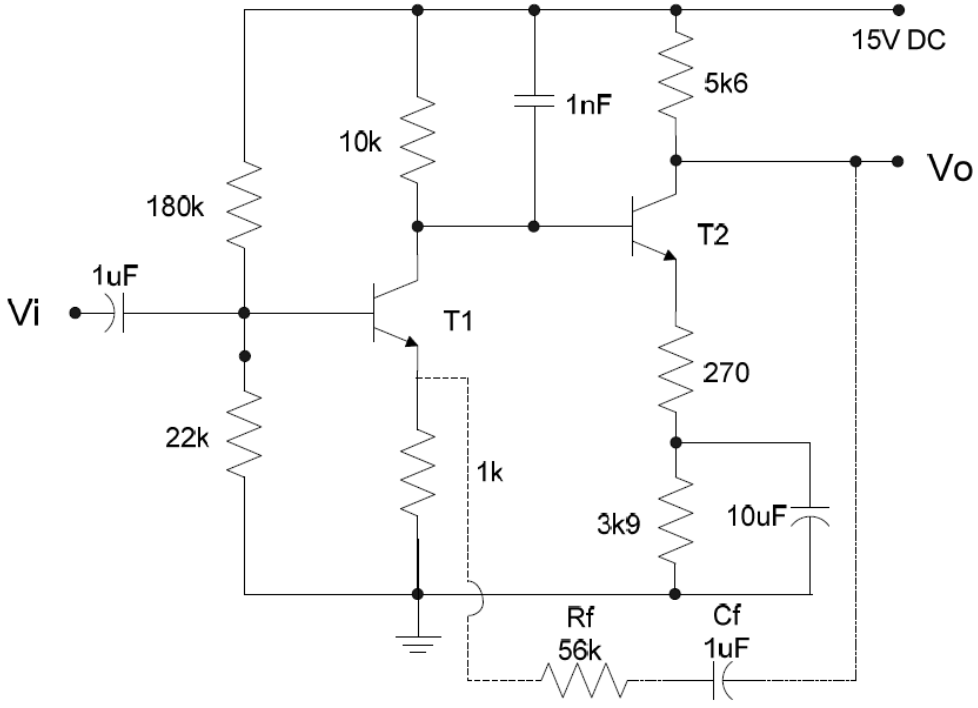
- M. S. Türköz, Elektronik, Birsen Yayınevi, İstanbul, 2004.
- D. Leblebici, Elektronik Devreleri, İTÜ Matbaası, 1992.
- Sedra & Smith, Microelectronic Circuits (5th Ed.), Oxford University Press, 2003.

EXPERIMENT 4

Feedback Transistor Amplifiers

Preliminary Work

- **Topics to be researched**
  - What is the feedback
  - What are the types of feedback, How does it affect the circuit according to the type of feedback?
  - What are the lower and upper cut-off frequency, how is it calculated?
- **Theoretical Calculation**
  - Calculate the DC operating point, gain and input-output resistances for the circuit in figure.(calculations will be made for normal and feedback situations)
- **Pspice Simulations**
  - Determination of the DC operating point of the circuit.
  - Determination of the gain for normal and feedback situations.[dB](Vo/Vi)
  - Determine the input-output resistances.



T1,T2: BC238C, hFE=230, hfe=330, hoe=20uA/V, fT=120MHz, Ccb'=2.5pF

Note: The part of the " Topics to be researched" is not requested in writing and it will not be taken before the experiment.You should study this part for better understanding of the experiment.Theoretical calculations and PSpice simulations are necessary.The preliminary work will be taken before the experiment.Before or during the experiment is expected to be successful in the written or the oral examination.

PURPOSE: Feedback which have wide range of applications in electronics, is obtained from the amplitude of the output signal of the system and this signal with the same property as the input signal is applied to the input of the system. In this experiment the effects of the feedback will investigate.

PRELIMINARY INFORMATION: Generally the input signal size, the output signal size and the transfer function of an amplifier defined as a_1, a_2, $A=a_2/a_1$, respectively. a_1 and a_2 can be current or voltage. A can be unitless, impedance or admittance.

If the amplitude $a_f=\beta a_2$ related to the a_2 output amplitude add to a_1, the feedback is applied to the circuit. β can be unitless, impedance or admittance. The block diagram of a feedback is given in figüre 1. Related to this;

$$a_f = \beta \, . \, a_2 \tag{1}$$

$$Af = \frac{a2}{a1} = \frac{A}{1-\beta A} \tag{2}$$

A_f is the transfer function of the feedback amplifier. A and β are related to the frequency. When we compare $|A_f|$ and $|A|$, there are two conditions. If $|A_f| < |A|$ namely $|1- \beta A|<1$, there are positive feedback. The positive feedback generally not use in electonic circuits apart from some speciel purpose.(pulse shapers, oscillators, active filters).

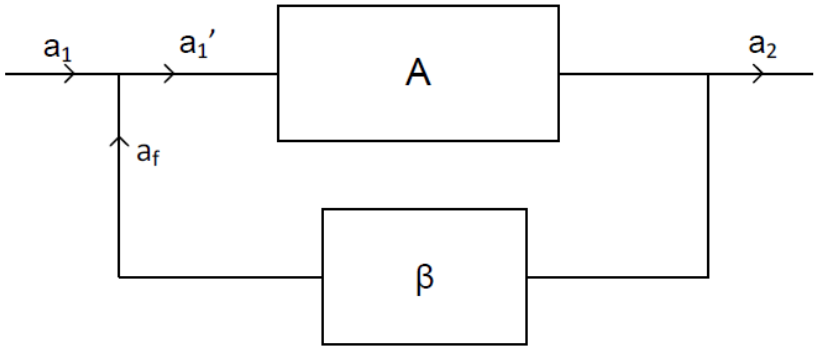


Figure 1: Feedback system block diagram

It can be extracted some important solution from equation 2.

- A_f is related to the amplitude and the sign of βA
- $\beta A = 0 \Rightarrow A_f = A$ and there is no feedback.
- $\beta A < 0 \Rightarrow A_f < A$ and there is negative feedback.
- $\beta A > 0 \Rightarrow A_f > A$ and there is positive feedback.
- $\beta A = 1 \Rightarrow A_f = \infty$ and the circuit oscillates.

If the logarithmic derivative of the equation 1 is taken, the change in A amplitude is reflected to the A_f by diminishing 1- βA rate. reduces the impact of changes in the properties of the active elements in the circuit.

Hormonic distortion etc. effects which don't related directly to the input signal can be formed in the active component. In this condition a_2= A.a_1' +a_3. From figure 1;

$$a2 = \frac{1}{1-\beta A} a1 + \frac{1}{1-\beta A} a3 \quad (3)$$

According to this the noise and the distortion at the output of the negative feedback circuit is lower than the no feedback circuit.

If the A_f transfer funciton of one pole circuit analyzed according to the frequency, the circuit which applied negative feedback system's upper cut-off frequency is higher and lower cut-off frequency is lower than the no feedback system. The input impedance or input admittance of a negative feedback circuit which input amplitude is voltage mode increses by $1 - \beta A$. The output impedance or output admittance of a negative feedback circuit which output amplitude is voltage mode decreases by $1 - \beta A$.

There are four type feedback;

- serial voltage feedback
- serial current feedback
- parallel voltage feedback
- parallel current feedback

References:

1. M. S. Türköz, Elektronik, Birsen Yayınevi, İstanbul, 2004.
2. Sedra & Smith, Microelectronic Circuits (5th Ed.), Oxford University Press, 2003.

EXPERIMENT 5

Characterization of PLL Basic Building Blocks

PRELAB STUDY

- Read through the experiment text and refered referances herein
- Review CD 4046 (PLL integrated circuit) data sheets
- Review XR 2228 (Multiplier integrated circuit) data sheets
- Calculate the cutoff frequency of Low Pass Filter (LPF) (In Fig. 5.8, assume R= 2.2k, C=2.2 uF)

ATTANTION

- **Prelab study** will be exemined at the begining of the lab session. You will take a **Quiz**.
- A supplementary measurement **document** will be provided in lab.
- Please remember all block diagrams except LPF are active circuits; they require decent **Power Supplies**

Aim of Experiment

The aim of this experiment is to characterize each PLL building block and verify PLL frequency tracking property.

Introduction

A Phase-Locked Loop (PLL) is a frequency tuning complex circuit. It can track variation of an input frequency in a range. Any information that has been encoded can be recovered by the PLL. The PLL itself is a fundamental building block of communication and instrumentation systems. FM Demodulation, Frequency Synthesis, Analog Digital Converters, Motor-Speed Control… are some to name.

To get familiar with the subject, first, PLL tracking property will be verified. Then, its capture and lock range will be determined. Finally, the characteristic properties of each block will be measured and mathematical model will be derived.

Fundamentals Building Blocks of PLL

A PLL has three fundamental blocks (circuits):

- **Voltage Controlled Oscillator**
  The oscillator output frequency is controlled with the input voltage (V_k). For zero input voltage, it runs at free-running frequency (f_o). The free running frequency can be controlled with an external capacitor.
- **Multiplier**

A multiplier has two input and one or two output terminals. It multiplies two incoming signals (V_{x1}, V_{x2}) and outputs the multiplication result (V_m). Analog and digital multipliers are available.

- **Low Pass Filter (LPF)**
  LPF smooth out multiplication result and provides a voltage proportional with phase difference of both signals (one is external input signal; the other is VCO output signal). This is voltage that is fed to VCO to synchronize both external input and VCO frequencies in lock range.

In addition to fundamental blocks, some application specific additional blocks may be included in the loop such as amplifier, prescaler and so on.

Note: The phase detector in the literature comprises the both multiplier and LPF

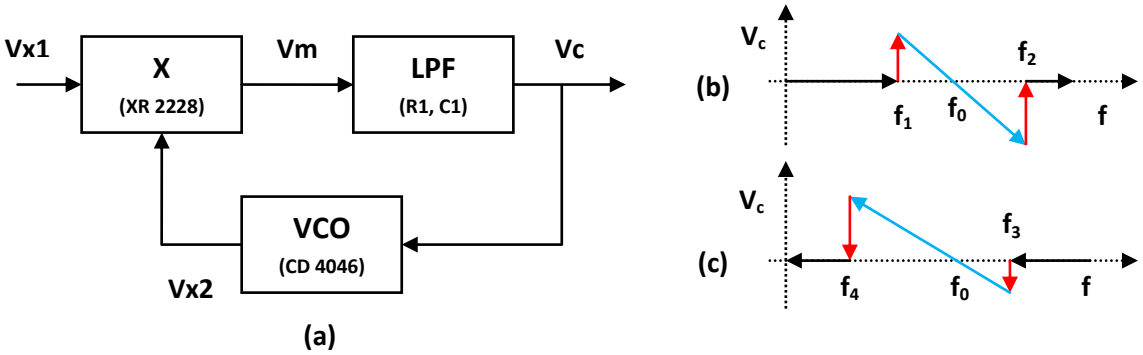


Fig 5.1 A fundamental PLL structure and frequency tracking processes

How does a PLL work?

Case#1: Increasing Frequency (Fig. 5.1.b)

Assume that the external input frequency is set to initial value that is very low in comparison to VCO free running frequency ($\mathbf{f_{x1} << f_0}$). And assume that the external input frequency has been increased from its initial value. When $\mathbf{f_{x1}}$ approaches to VCO free running frequency up to LPF cutoff frequency [$\mathbf{f_{x1} \sim (f_0 - f_h)}$], the PLL locks the input signal frequency at $\mathbf{f_1}$. Both inputs will have the same frequency ($\mathbf{f_{x1} = f_{x2}}$) with a phase difference ($\mathbf{\emptyset}$) in between. If one continues to increase the external input frequency; the PLL flows that frequency up to an $\mathbf{f_2}$ frequency. Further increasing of external frequency will break down the loop. After $\mathbf{f_2}$ frequency, the VCO will run around of its free running frequency ($\mathbf{f_0}$) and LPF output will be irrelevant.

Case#2: Decreasing Frequency (Fig. 5.1.c)

Assume that the external input signal is set to a frequency very large in comparison to the free running frequency of VCO ($\mathbf{f_{x1} >> f_0}$). And assume that the external input frequency has been decreased. When the $\mathbf{f_{x1}}$ approaches to $\mathbf{f_0}$ [$\mathbf{f_{x1} \sim (f_0+f_h)}$], the PLL will lock again at the $\mathbf{f_3}$ frequency. Both inputs of multiplier will have the same frequency ($\mathbf{f_{x1} = f_{x2}}$) with a phase difference in between

(**Ø**). The lock process flows up to $\mathbf{f_4}$ frequency. Further decreasing the external input frequency will break down the loop. After the break down the VCO again run around its free running frequency ($\mathbf{f_0}$) and LPF output will be irrelevant.

PLL Lock and Capture Ranges

As stated above, tracing the increasing frequency range will provide $\mathbf{f_1}$ and $\mathbf{f_2}$ frequencies with their associated control voltages ($\mathbf{V_{c1}}$, $\mathbf{V_{c2}}$). In order to capture the external input signal for the first time, the external input frequency ($\mathbf{f_{x1}}$) should be close to VCO free running frequency ($\mathbf{f_0}$) enough, say $\mathbf{f_h}$.

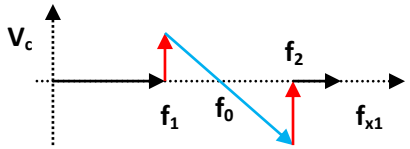


Fig 5.2 PLL lock process in increasing frequencies.

For increasing frequency, the capturing process starts around of $\mathbf{f_{x1} \sim (f_o - f_h)}$

Tracing the decreasing frequency range will provide $\mathbf{f_3}$ and $\mathbf{f_4}$ frequencies with their associated control voltages ($\mathbf{V_{c3}}$, $\mathbf{V_{c4}}$).

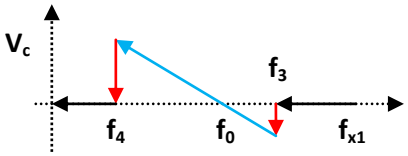


Fig 5.3 PLL lock process in decreasing frequencies.

For decreasing frequency, the capturing process starts around of $\mathbf{f_{x1} \sim (f_o + f_h)}$

The difference between first capture frequencies ($\mathbf{f_1}$ and $\mathbf{f_3}$) for both increasing and decreasing processes is called **capture range**. For the current example, the capture range is ($\mathbf{f_3 - f_1}$)

The difference between loop breaking frequencies ($\mathbf{f_2}$ and $\mathbf{f_4}$) for both increasing and decreasing processes is called **lock range**. For the current example, the lock range is ($\mathbf{f_2 - f_4}$)

Assume the followings characteristics for a PLL

- VCO Gain: K_O
- Phase Detector Gain: K_d
- LPF Elements: R and C

The measurements will provide the followings,

- **Capture Range:** $\Delta f_C = (f_3 - f_1)$ (5.1)
- **Lock Range :** $\Delta f_l = (f_2 - f_4)$ (5.2)

The theoretical calculation of the PLL at hand will provide the followings,

- **Capture Range :** $\Delta f_C = [(K_O * K_d)/(R * C)]^{1/2}$ [Hz] (5.3)
- **Lock Range :** $\Delta f_l = K_O * K_d$ [Hz] (5.4)
- **For all PLL:** $(f_3 - f_1) < (f_2 - f_4)$

Because of nonlinearity nature of the loop and difficulties in determination of all stated frequency components, the theoretical and measurement values may not agree well.

Measurement Main Steps

The Fig. 5.1a block diagram will be used in measurements. Multiplier and VCO blocks are complex circuits. They should be connected to the proper power supplies.

(1) Use a sine wave oscillator as V_{x1}
(2) Use a DC voltmeter to measure V_c
(3) Use an oscilloscope to display V_{x1} and V_{x2} signals
(4) Use a frequency-meter to measure oscillator frequency
(5) Follow the steps in the supplementary sheets

Characterization of Voltage Controlled Oscillator

A Voltage Controlled Oscillator (VCO) converts a voltage at its input to a frequency at its output. It is a simply a voltage to frequency converter. Output waveform is not a main concern. For the IC at hand, it has a square waveform.

The characterization measurements provide parameters for mathematical model of VCO.

The mathematical model of a VCO is as follows

- $f = K_o * V_c + f_0$ (5.5)

Characteristic parameters are:

K_o : Voltage to frequency conversion gain
f_0 : Free running frequency

It is desirable to have a device with linear characteristics as much as possible.

Measurement Main Steps

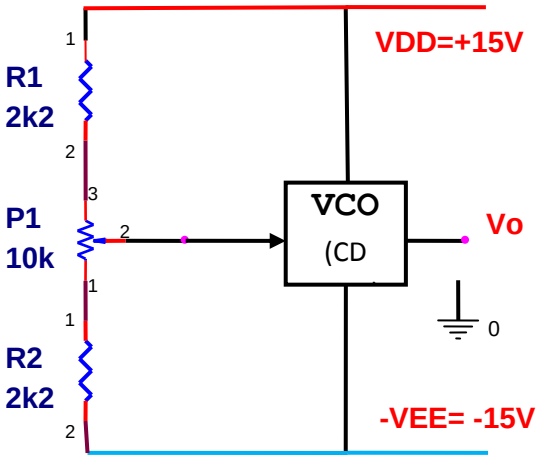


Fig 5.4 VCO measurement circuit

(1) Use P1 potentiometer to set input voltage
(2) Use a DC Voltmeter to measure input voltage
(3) Use an oscilloscope to display output
(4) Use a frequency-meter or oscilloscope to measure output frequency
(5) Follow the steps in supplementary sheets
(6) Plot frequency versus voltage
(7) Calculate characteristics (K_o, f_o)

Characterization of Phase Detector

(Phase Detector: Multiplier + LPF)

A multiplier multiplies two signals at its inputs and outputs the result. A LPF at output of multiplier suppresses the high frequency products and passes low frequency products (the phase component) within the pass band. To clarify phase detection process the following two examples are presented.

Example#1

Assume the following input signals:

$V_{x1} = V_{m1} \cos(w_1 t)$

$V_{x2} = V_{m2} \cos(w_2 t + \phi)$

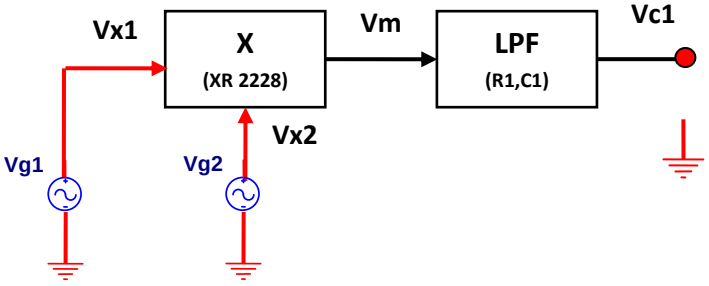


Fig 5.5 Phase detector (Multiplier + LPF).

The following products will appear at the output of the multiplier:

$$V_m = k \cdot (V_{m1} \cdot V_{m2} /2)[\cos((w_1 - w_2)t - \phi) + \cos((w_1 + w_2)t + \phi)]$$

In a locked PLL, $w_1 = w_2 = w$ is always satisfied. Under this assumption the multiplier output will be as follows,

$$V_m = k \cdot (V_{m1} \cdot V_{m2} /2)\,[\cos(\phi) + \cos(2wt + \phi)]$$

The high frequency term, (2 w) will be suppressed by the LPF. The low frequency term will appear at the output of the LPF.

The LPF output will be as follow,

$$V_c = k \cdot [(V_{m1} . V_{m2})/ 2] \cdot \cos(\phi)$$

(5.6)

The LPF will provide a voltage related to phase difference of two input signals. It is important to note that the output voltage and phase difference relation is not a linear relation.
$V_k = F(\phi)$ is non-linear.

The phase detector gain is defined as follow,

$$K_d = k \cdot (V_{m1} \cdot V_{m2})/ 2 \qquad (5.7)$$

It is clear that the phase detector gain depends on the input signal amplitudes. To fix the detector gain, the multiplier circuit should be operated in the saturation mode.

The mathematical model of PD,

$$V_c = K_d \cdot \cos(\phi) \qquad (5.8)$$

Example#2

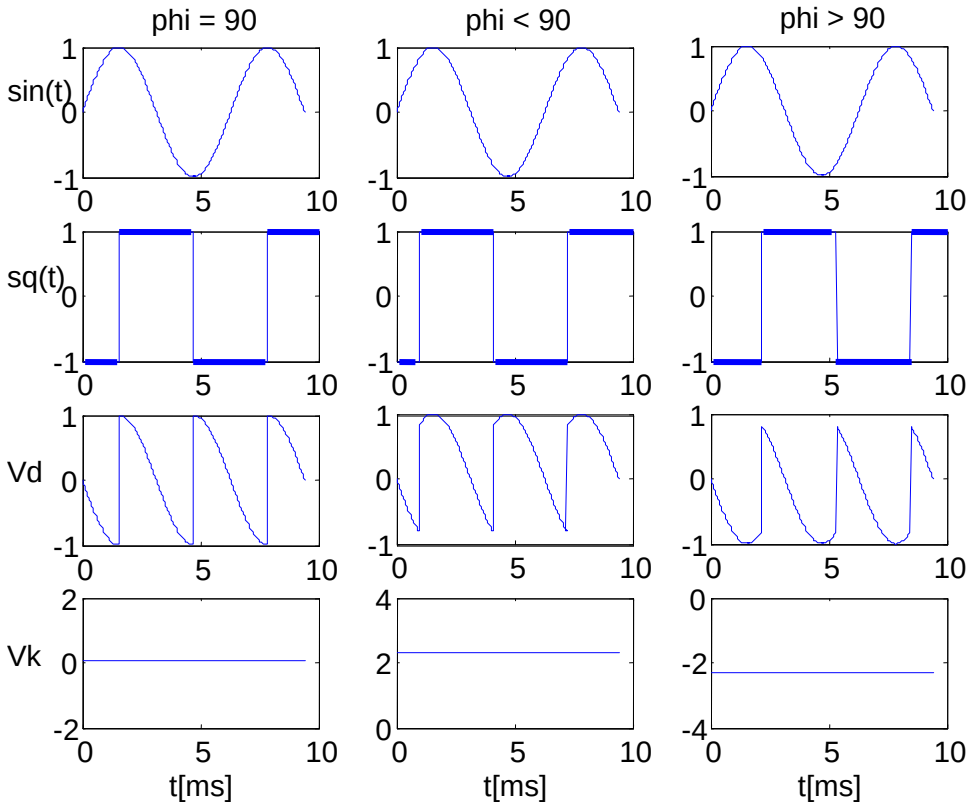
The following example is for to clarify the operation of the phase detector.

Assume the following signals at inputs of analog multiplier:

$V_{x1} = 1^* \sin(w\,t)$

$V_{x2} = 1^* \text{square}(w\,t + \phi)$

The multiplication of these two signals is simulated in MATLAB™. And the results are presented as follows,



(a) $\phi = 90^\circ$ (b) $\phi < 90^\circ$ (c) $\phi > 90^\circ$

Fig 5.6 Simulation of a Phase Detector.

- Row#1 figures present sine wave at input#1. It is kept fixed as a reference.
- Row#2 figures present square wave with 3 different phase differences with respect to sine wave.
- Row#3 figures present multiplication result of two signals.
- Row#4 figures present output of LPF, integration of multiplication result
- The each column presents a particular phase difference.

The simulation presents a locked PLL. Since an unlocked PLL is out of context, it is not discussed here.

Measurement Main Steps

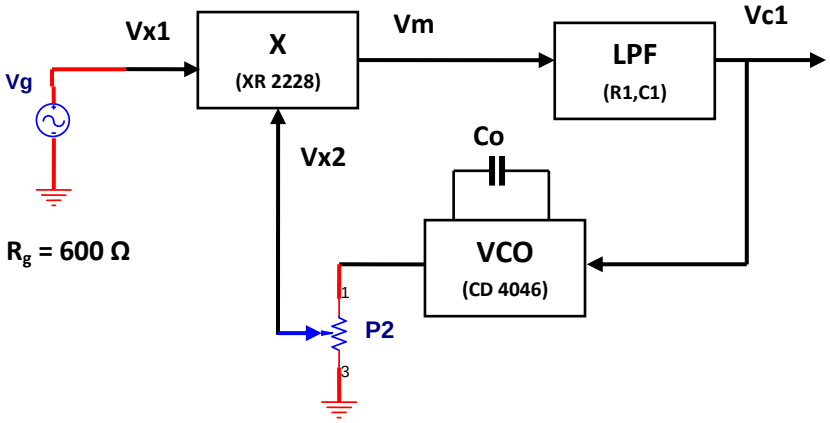


Fig 5.7 Phase Detector (PD) measurement circuit.

In this indirect method, the phase difference will be measured on oscilloscope and control voltage will be measured with a DC voltmeter. All measurements should be made when PLL is in lock. Because the method is involved the care must be taken.

(1)First of all, put PLL in lock condition
(2)Connect sine wave to CH#1 and square wave to CH#2 of oscilloscope

(3) For **Ø = 90°** phase difference:

To get Fig. 5.9(a) display, set the **frequency** and **amplitude** of the oscillator accordingly.
Typical values are: $\mathbf{V_{x1}(pp) \sim 3\ V}$, $\mathbf{f_{x1} \sim 5\ kHz}$ for sine wave and $\mathbf{V_{x2}(pp) \sim 4\ V}$ for square wave.
Measure $\mathbf{X_0}$ difference and record $\mathbf{V_k}$ control voltage. An offset voltage may appear.

(4) For **Ø < 90°** phase difference:

To get Fig. 9(b) display, change the oscillator **frequency**. Measure $\mathbf{X_1}$ difference and record $\mathbf{V_k}$ control voltage. Repeat the procedure for four different frequencies to get four different X_1 values.

(5) For **Ø > 90°** phase difference:

To get Fig. 9(c) display, change the oscillator frequency accordingly. Measure $\mathbf{X_2}$ difference and record $\mathbf{V_k}$ control voltage. Repeat the procedure for four different frequencies to get four different $\mathbf{X_2}$ values.

(6) Follow the steps in supplementary sheets
(7) From above measurements calculate the exact phase differences in radians.
(8) Plot the voltage versus the phase difference.
(9) Calculate a typical phase detector gain (K_d) around of **Ø = 90°** phase difference.

Characterization of Low Pass Filter

The LPF suppresses loop high frequency products in lock process. And as a result, it is a dominant factor in determination of the capture range.

The main characteristics of an LPF in context of PLL are as follows

- Module of voltage transfer function

$$H(f) = \frac{1}{\sqrt{\left(1+\left(\frac{f}{f_c}\right)^2\right)}} \quad (5.9)$$

- Cutoff frequency (Hz):

$$f_c = \frac{1}{2\pi RC} \quad (5.10)$$

- Attenuation (dB) after the cutoff

$$-20 \cdot log\left(\frac{f}{f_c}\right) \quad (5.11)$$

- Phase shift (rad)

$$\emptyset = -arctg\left(\frac{f}{f_c}\right) \quad (5.12)$$

Measurement Main Steps

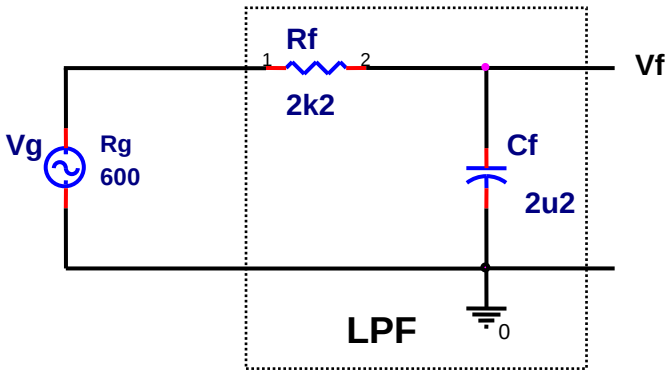


Fig 5.8 LPF measurement circuit

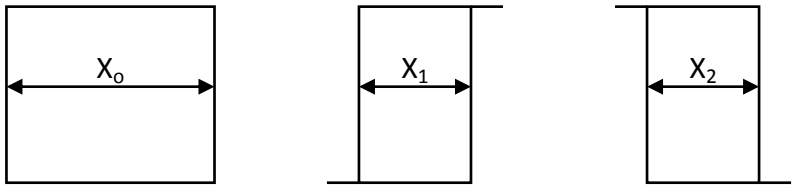
(1) Use a sine oscillator at input
(2) Set frequency and amplitude of oscillator to proper values
(3) Use an AC Voltmeter to monitor input voltage
(4) Use an AC Voltmeter to measure filter output in dB
(5) Use an Oscilloscope to display input and output
(6) Record the filter output voltage as sine oscillator frequency is swept in decades
(7) The filter input voltage always should be kept constant at its initial value.
(8) Follow the steps in the supplementary sheets
(9) Plot the measurement result in a semilog scale (frequency in log scale, voltage in linear scale)
(10) Calculate the characteristics (f_h and attenuation)

APPENDIX-A

Measurement of Phase Difference in Between Sine and Square Waves

In general, the measurement of phase difference of two signals of the same frequency on oscilloscope requires some labor. First, each signal should be connect to the one channel. Then, both channels should be triggered so to get a stable display. After that, the oscilloscope should be switched to XY- mode. Finally, from display measurement one can calculate the phase difference. In literature, in case of two sine signals, the XY-displays are known as Lissajous figures. In case of sine and square waves, the figures and formulas are derived in ITU lab.

In case of sine (in CH#1) and square waves (in CH#2), one gets the following displays for various phase differences. As frequency of sine is changed independently, the PLL follows that change with a phase difference. Then one gets the following deformed displays. Therein, one can calculate the phase differences.



(a) $\Delta = 90^o$ (b) $\Delta < 90^o$ (c) $\Delta > 90^o$

Fig. 5.9 Sine and square waves displays for different phase in oscilloscope XY operation mode.

X_o : The distance in between deforming sides (not deformed yet) of the rectangle for 90 degree phase difference.
X : The distance in between deformed sides of the rectangle for phase difference different than 90 degree

Δ : The deformation amount

$$\Delta = X_o - X \quad (5.13)$$

For **Ø < 90°** phase difference,

Phase difference: $\phi = 90 - [(\Delta/X_o) \times 90]$ [degree] (5.14)

For **Ø > 90°** phase difference,

Phase difference: $\phi = 90 + [(\Delta/X_o) \times 90]$ [degree] (5.15)

Phase difference conversion to radian,

$$\emptyset(rad) = \frac{[\emptyset(degeee)]}{360} \times 2\pi \quad (5.16)$$

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[1] ITU, "Yüksek Frekans Laboratuvarı Deneyleri", Ed.3, ITU, 1984.
[2] WILLIAMS, Arthur B., "Designer's Handbook of Integrated Circuits", McGraw-Hill, (1984).
[3] GREBENE, Alan B., "Bipolar and MOS Analog Integrated Circuit Design", (1984).
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[5] Tietz, U, and Schenk, Ch, "Electronic Circuits", Springer, 1991.
[6] www.google.com, Key words: PLL, PLL Characterization.

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EXPERIMENT 7
Low Frequency Oscillators

Preparation

Subjects to study before the experiment day

- What is Barkhausen criterion?
- What is the oscillation frequency of the sinus oscillator? Investigate the relation of this frequency to the amplitude and phase of the total loop gain in the sinusoidal steady state.

Theoretical Calculations

- As it is seen from Figure 2, Feedback circuit is operating as a high pass filter with three poles. Is it possible to realize a sinus oscillator replacing the resistances and capacitors in the β circuit?
- Prove the oscillation frequency expressions of the circuits in Figure 3, Figure 7 and Figure 9.

Circuit Analysis using SPICE

- Set up the circuit in Figure 3 in SPICE environment. Make the circuit to oscillate using the potentiometer. Draw the signals at nodes 1,2 and 3 for the case that there is no clipping in sinus signal.
- Set up the circuit in Figure 6 in SPICE environment. Using time domain analysis of the circuit, draw the signals at nodes 1,2 and 3.
- Set up the circuit in Figure 8 in SPICE environment. Using time domain analysis of the circuit, draw the signals at nodes 1,2 and 3.

Note: The part "**Subjects to study before the experiment day**" is not obligatory to be given as a written report however it should have been studied before the experiment to understand the subjects more clearly. The study about the parts "**Theoretical Calculations"** and **"Circuit Analysis using SPICE"** will be taken and it will be graded as prior study**.**

Purpose

In this experiment, low frequency oscillators will be explained and their circuit applications will be demonstrated.

Introduction

Oscillators are classified according to the wave forms they produce. Therefore, oscillators which produce sinus signal are called as sinus oscillators. There are several sinus oscillators in the literature. The important features expected from a sine oscillator are frequency stability, signal amplitude stability, and how much the signal it produce, resembles a sinus waveform.

In the first part of the experiment, phase-shift oscillator will be discussed in order to examine the operating principles of sinus oscillators. However, before proceeding to the analysis of these oscillator circuits, it is useful to mention some of the important criteria for oscillation. Since this issue is discussed in detail in Analog Electronic Circuits course, we will explain some of the important subjects briefly here.

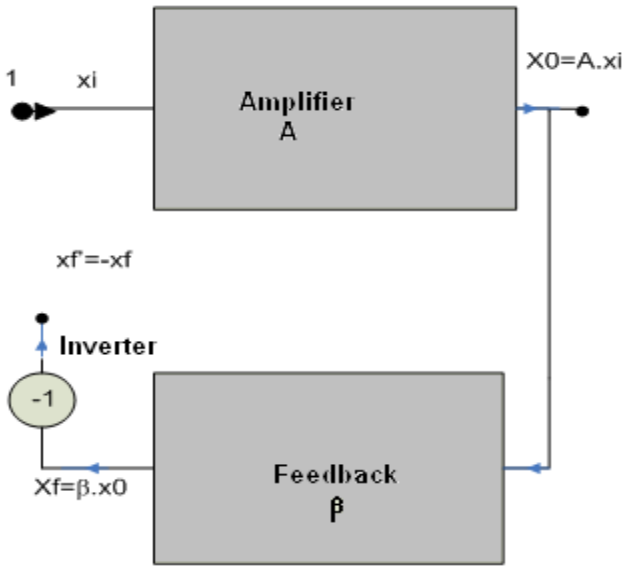


Figure 1. Block diagram of the feedback applied circuit

An amplifier and a feedback circuit are shown in Figure 1. At the output of the amplifier, $\mathbf{x_o}$ signal is produced according to the $\mathbf{x_i}$ input signal. The output of the feedback circuit becomes $\mathbf{x_f} = \boldsymbol{\beta} x_o = \boldsymbol{\beta A} x_i$ and inverter output becomes $\mathbf{x_f'} = -\mathbf{x_f} = -\mathbf{A}\boldsymbol{\beta} x_i$

From Figure 1, loop gain:

$$(xf' / \mathbf{x_i}) = -\mathbf{x_f} / \mathbf{x_i} = -\boldsymbol{\beta}\mathbf{A}$$

Now let's think the conditions that the output source signal $\mathbf{x_f'}$ **and** $\mathbf{x_i}$ are at the same phase and amplitude. In this case, if we remove externally applied source signal and connect the node 2 to node 1, $\mathbf{x_o}$ amplifier output signal will continue to be the same.

Phase-Shift Oscillator

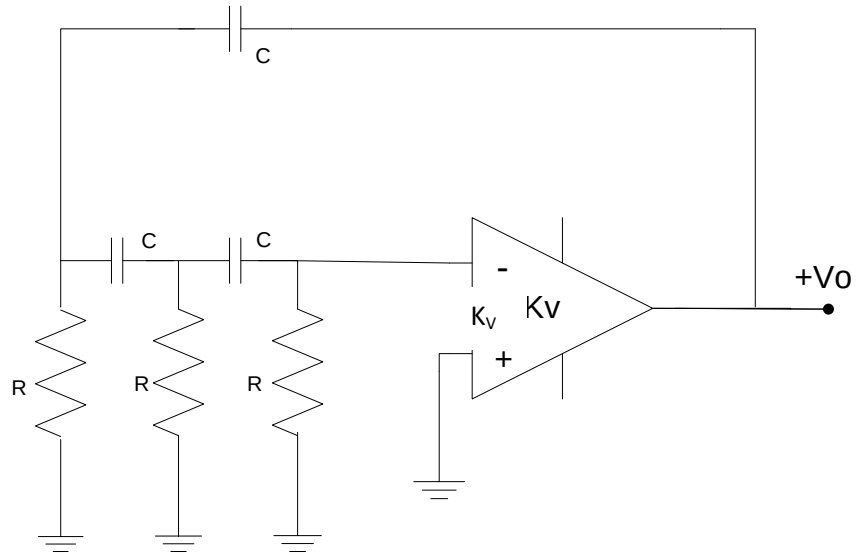


Figure 2. General Structure of Phase-Shift Oscillator

In Figure 2, general structure of phase-shift oscillator is depicted. This phase-shift oscillator is generated using a feedback circuit consisting of an inverting amplifier, resistance and capacitance elements.

Sinusoidal steady-state analysis gives, as α= 1/ωRC :

$$-\beta(j\omega) = \frac{Vi(j\omega)}{Vo(j\omega)} = \frac{1}{1 - 5\alpha^2 - j(6\alpha - \alpha^3)} \qquad (1)$$

For oscillation ∠ [Aβ(jω)]= 0° we remember ∠ [Aβ(jω)]+ ∠ [A]= ∠ [β(jω)]+180° (A=-K_V, 180° inverting amplifier) the frequency that RC circuit gives phase-shift of 180° is the oscillation frequency.

$$f = \frac{1}{2\pi RC\sqrt{6}} \qquad (2)$$

It can be found that [β(jω)]=1/29 at the oscillation frequency. According to [Aβ(jω)] ≥1 condition, [A] ≥1/β(jω) results in **[A] ≥29**. Practically, total loop gain amplitude is chosen as greater than one (for example %5). Hence, the amplitude of the sinus signal at the output will be multiplied in each loop by a gain of higher than one. This results in a continuously growing sinus signal at the output which however is limited by the non-linearity of the inverting amplifier. This limitation becomes more significant for large amplitude signals and at the boundaries of clipping. Therefore the amplitude of the output sinus signal becomes a bit less than the clipping conditions of the amplifier.

As it is seen from the Figure 2, feedback circuit is operating as a three-pole high pass filter. Figure out if it is possible to generate a sinus oscillator by replacing the places of resistances and capacitors.

Set up the circuit in Figure 3. Make the circuit to oscillate using R' potentiometer (while doing this, try to minimize the clipping of the sinus wave). During adjustments, investigate the clipping and the pace of the diminishing sinus signal time to time. For the minimum clipping case, draw the signal waves at the nodes 1,2 and 3.

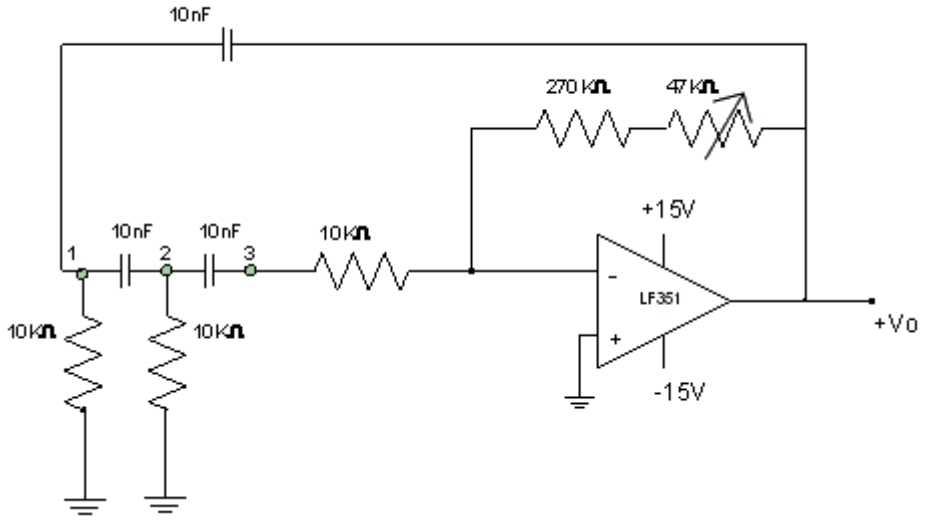


Figure 3. Phase-Shift Oscillator

Charge-Recharge (Relaxation) Oscillators

Charge-Recharge based oscillators usually produce square, triangular and zigzag wave types. Operating principle of these types of oscillators are different from the aforementioned sinus oscillators. Therefore, the analysis of these types of oscillators will be different.

The oscillators whose operating principle based on a capacitor charge-recharge are called charge-recharge (relaxation) oscillators. These oscillator circuits usually employ Schmitt triggers as active elements

A Schmitt trigger circuit realized with an operational amplifier is shown in Figure 4. Looking at Figure 4a, suppose $v_i < v_1$. In this case, $v_0=+V_0$ (for example +5V). As a result of the analysis from Figure 4a:

$$v1 = +\frac{VRR1}{R1+R2} + \frac{V0R2}{R1+R2} = V1 \qquad (3)$$

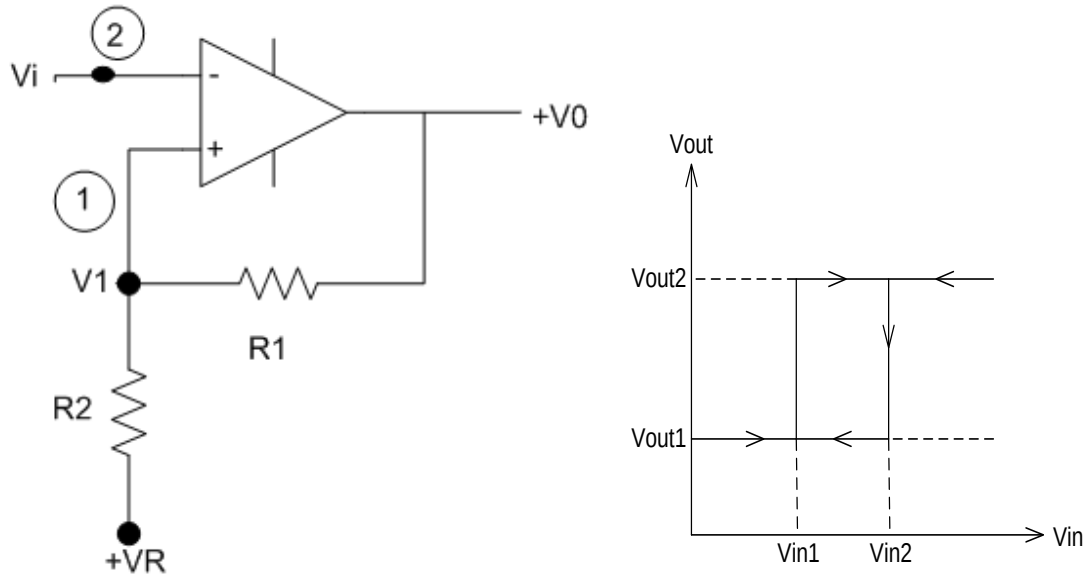


Figure 4 (a). Schmitt trigger circuit **4 (b).** Input output characteristics of Schmitt trigger circuit

If v_i increases, under the condition of $v_i < v_1$, v0 remains constant at the value $+V_0$. At the same time $v_i=V_1$ remains constant. This situation continues until voltage $v_i=V_1$. At this critical threshold output voltage v_0, suddenly jump to the value of $-V_0$. Output voltage will keep this value as long as $v_i>V_1$. When $v_i>V_1$, v_1 voltage will change and its value will become:

$$v1 = +\frac{R1VR}{R1+R2} - \frac{R2V0}{R1+R2} = V2 \qquad (4)$$

When $v_i>V_1$ if $V_{i\ voltage}$ is started to be reduced, output voltage will remain constant at $-V_0$ value until the condition $v_i=V_2$ is satisfied. When $v_i=V_2$ condition is satisfied, output voltage will jump to the $+V_0$ voltage value. Thus the initial state is revisited and the cycle will continue in this way.

The difference between the voltages V_1 and V_2 is called hysteresis and it is indicated by V_H.

$$VH = V1 - V2 = \frac{2R2\ V0}{R1+R2} \qquad (5)$$

Graphical representation of the studies about Schmitt trigger circuit made so far is shown in Figure 4b.

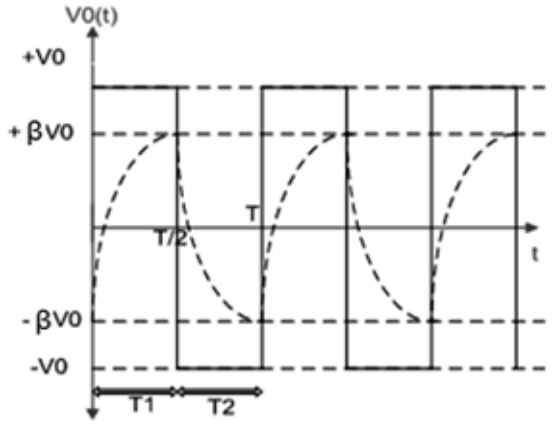
RC Charge Recharge Square-wave Oscillator

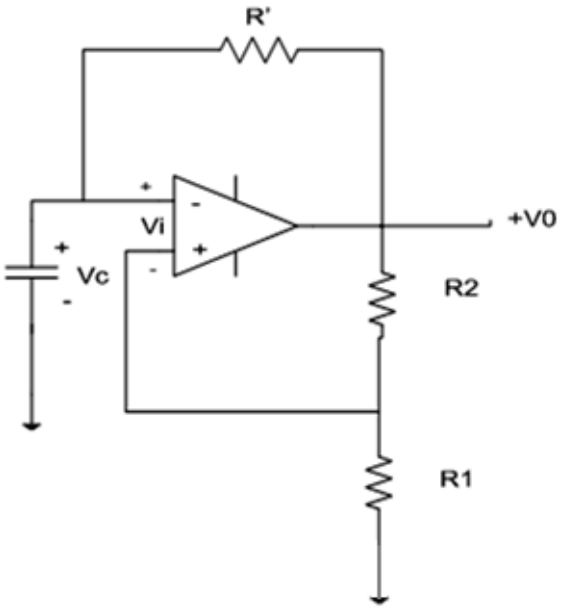
A square-wave oscillator is shown in Figure 5b. A Schmitt trigger realized by an operational amplifier is used in the circuit.

Operational amplifier's positive input terminal gets a specific voltage from the output with a rate of $\beta = R_1/(R_1 + R_2)$. Input differential voltage v_i (Figure 5b) can be written as:

$$v_i = v_c - \beta v_0 \qquad (6)$$

From the definition equations of operational amplifier, if input differential voltage vi is positive, the output voltage will be $v_0=-V_0$. Now let's think the condition when $v_i < 0$ or $v_c < \beta v_0=\beta V_0$ is satisfied at a specific time moment t. The voltage of C capacitor will increase via the resistor R' to the value $+V_0$ exponentially. During this period, output voltage v_0, will remain constant at the value $+V_0$ until the condition $v_c= \beta V_0$ is satisfied. When the condition $v_c= \beta V_0$ is achieved this stability will be disrupted and the output voltage will jump to the value $v_0 =-V_0$. While the output is at the value $-V_o$, the voltage of the operational amplifier's positive terminal will be $-\beta V_0$. Then, C capacitor will be discharged by R' resistance. Output voltage will remain at $-V_0$ value and operational amplifier's positive terminal voltage will continue to be at the value $-\beta V_0$ until $vc = -\beta V_0$. At this critical v_c value, output voltage will be $v_0 =+ V_0$, operational amplifier positive terminal will jump to $+\beta V_0$ voltage and initial condition will have been revisited. Described points are depicted in Figure 5a.





Figue 5 (a). Square-wave oscillator characteristic **Figure 5 (b).** Square-wave oscillator circuit

As a result of the analysis, the oscillation frequency of the circuit:

$$f = \frac{1}{2R'C \ln\{\frac{2R1 + R2}{R2}\}} \qquad (7)$$

More detailed analysis of this equation can be found in your Analog Electronic course notes or several textbooks.

Set up the circuit in Figure 6. Measure the oscillation frequency of the circuit. Compare this result with your calculated frequency. Draw the waveforms at nodes 1,2 and 3.

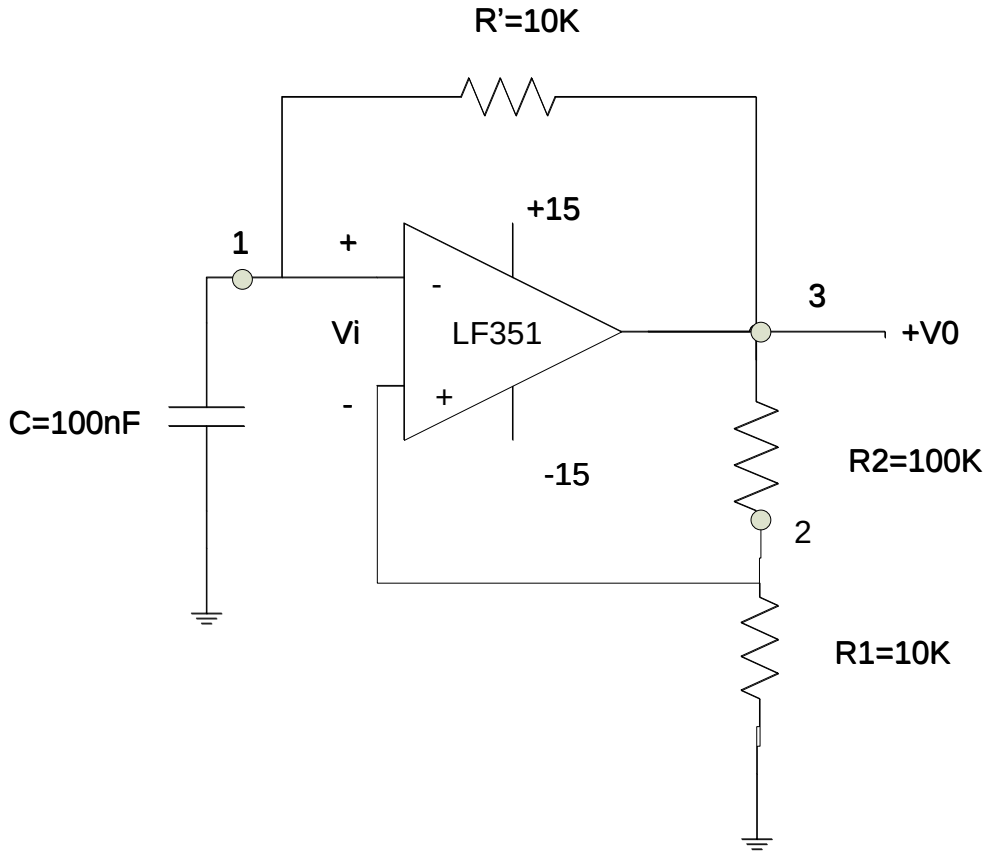


Figure 6. Square-wave oscillator circuit

Triangular-wave Oscillator

As it can be seen from Figure 5b, the waveform at the negative input of the comparator in the square-wave oscillator can be approximately considered as triangular wave when βV_0 value significantly smaller than V_0. However, recharge of a capacitor via a resistance is exponential so it is not appropriate to use this circuit as triangular-wave oscillator. Instead, oscillators that based on capacitor charging with constant current are designed. As it is known that if the capacitor is charged with constant current its voltage increases linearly. Similarly if the capacitor is discharged with constant current its voltage decreases linearly too.

To drive the capacitor with constant current, an integrator circuit is used in Figure 7a. Therefore, its output voltage changes linearly. Due to integrator circuit phase change, output node is connected to the positive terminal of the comparator.

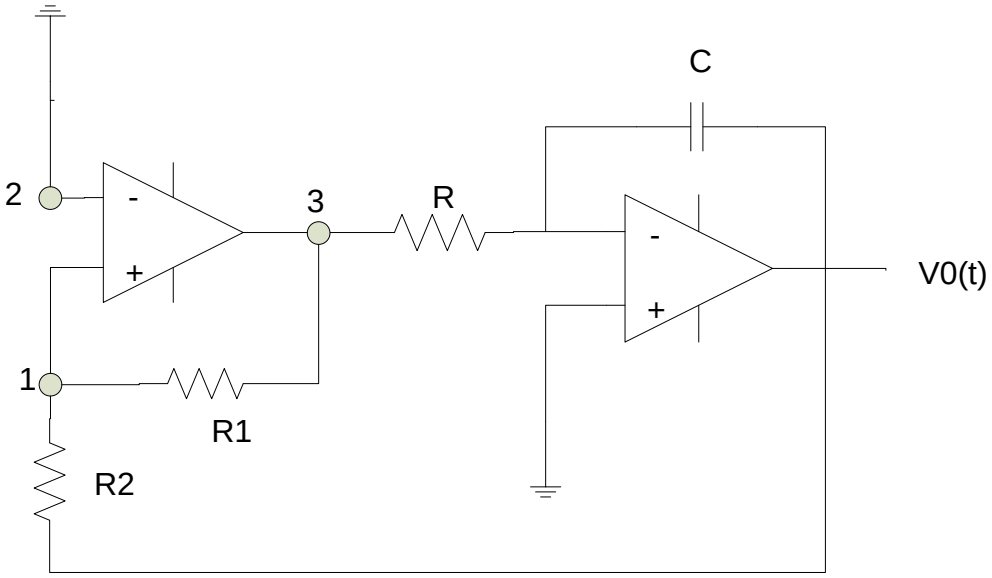


Figure 7 (a). Triangular-wave oscillator

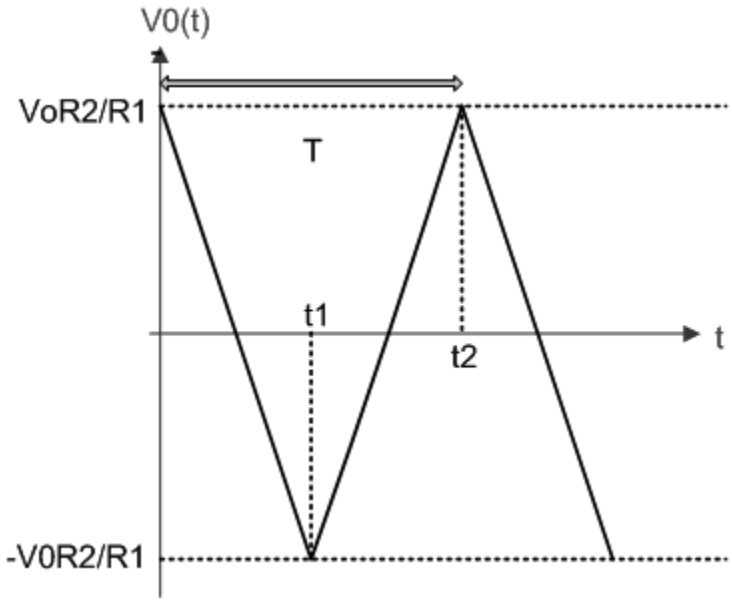


Figure 7 (b). Triangular-wave oscillator output characteristic

Now at t=0 moment, suppose Schmitt trigger output is at $+V_0$ voltage . In this case, the output of the integrator circuit becomes:

$$V0\ (t) = -\frac{1}{RC}\int_{t0=0}^{t} +V_0\ (t)dt \qquad (8)$$

as voltage changing linearly. For this case, if we name the node 1 voltage in Figure 7a as $V_1(t)$, it becomes:

$$V1(t) = \frac{R1v0(t)}{R1+R2} + \frac{R2V0}{R1+R2} \qquad (9)$$

Since the negative terminal of the operational amplifier is grounded, the voltage at the node 3 will jump to $-V_0$ when the node 1 voltage zero. If we name moment t_1 as this occurs, for $t= t_1$ and under $V_1(t)=0$ condition:

$$v0(t) = -\frac{R2}{R1}\,V0 \qquad (10)$$

At $t=t_1$ since node 3 voltage is $-V_0$, node 1 voltage becomes:

$$V1(t) = -\frac{R2V0}{R1+R2} + \frac{R1v0(t)}{R1+R2} \qquad (11)$$

if the node 3 voltage jump to $+V_0$ at time t_2 and under $V_1(t)=0$ condition, it becomes:

$$v0(t) = +\frac{R2}{R1}\,V0 \qquad (12)$$

Oscillation frequency of the circuit:

$$f = \frac{R1}{4RR2C} \qquad (13)$$

In the experiment, set up the circuit in Figure 8. Measure the oscillation frequency of the circuit. Compare this result with your calculated frequency. Draw the waveforms at nodes 1,2 and 3.

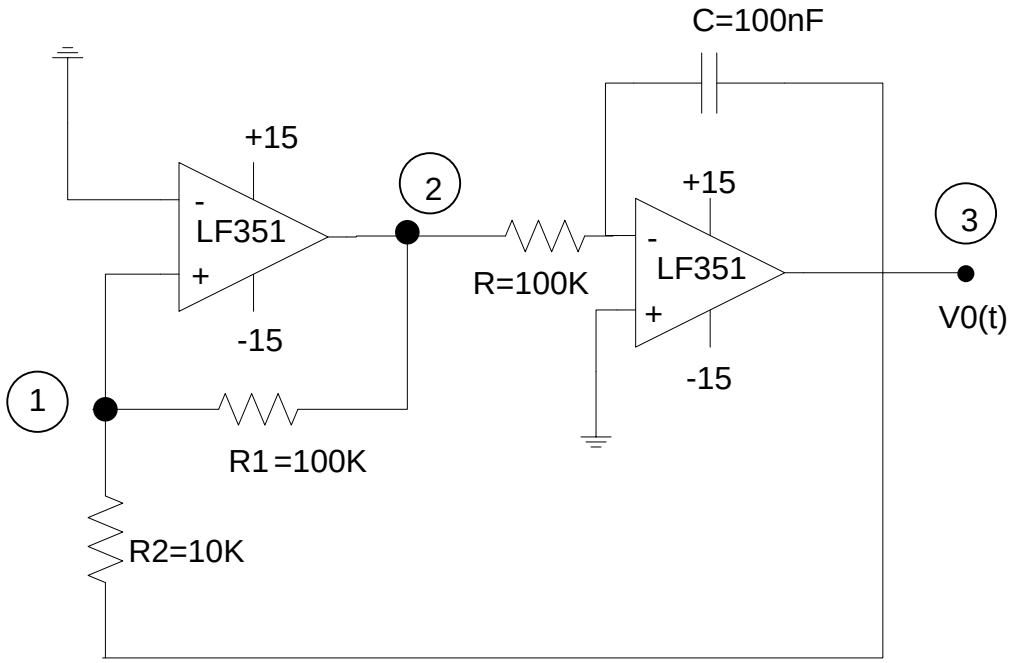


Figure 8. Triangular-wave oscillator

Things to do in the experiment

Experiment I

For the phase-shift oscillator circuit in Figure 3, using potentiometer, adjust for minimum clipping at the output. For this case, draw the waveforms at node 1, 2 and 3 in the lab paper you are given and attach this paper to your final lab report. Compare all your results with your theoretical calculations.

Experiment II

For the circuit in Figure 6, repeat the procedures that you have done for experiment I.

Experiment III

For the circuit in Figure 8, repeat the procedures that you have done for experiment I.

EXPERIMENT 8
Active Filters

Purpose:

Investigation the principle of the filters which are designed using active elements and examination the output voltages of filters for different input signal.

Preliminary Work

- **Topics to be researched**
  - Researh the differences between active filter and passive filter
  - Define the advantages of the active filter
  - Look for the application areas of the low-pass, high-pass and band-pass filters.
- **Theoretical Calculation**
  - Express the R_1,R_2,R_5 resistors in terms of H_0, f_0 and Q to use for band pass filter given in Figure 1b.(Equations are given in 2,3,4)
  - Express the R_3,R_4 resistors in terms of H_0, f_0 and Q to use for high pass filter given in Figure 2b.
  - Calculate R_1,R_2,R_5 values for the band pass filter.[H0=10,f0=20kHz and Q=5; C3=C4,the calculations will be done for 100pF,200pF and 270pF]
  - Calculate R_3,R_4 values for the high pass filter.[H0=1,f0=20kHz and Q=$1/\sqrt{2}$; C3=C4,the calculations will be done for 100pF,200pF and 270pF]
- **Pspice Simulations**
  - Determine the lower upper cut-off frequency and center frequency for the band pass filter in figure 1b.(Use the resistor values found in theoretical calculations)
  - Determine the lower upper cut-off frequency and center frequency for the high pass filter in figure 2b.(Use the resistor values found in theoretical calculations)

Note: The part of the " Topics to be researched" is not requested in writing and it will not be taken before the experiment.You should study this part for better understanding of the experiment.Theoretical calculations and PSpice simulations are necessary.The preliminary work will be taken before the experiment.Before or during the experiment is expected to be successful in the written or the oral examination.

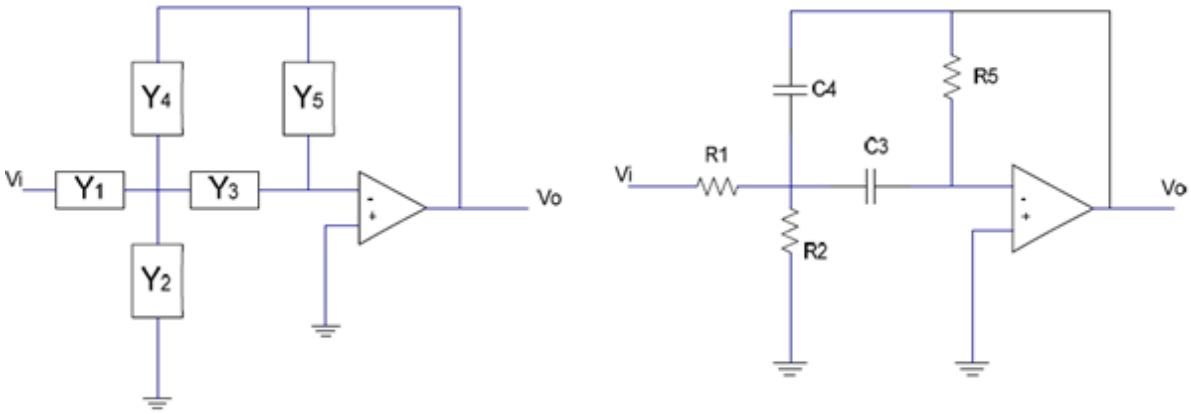
Experiment 1

$$\frac{V_o}{V_i} = \frac{-Y_1 Y_3}{Y_5(Y_1+Y_2+Y_3+Y_4)+Y_3 Y_4} \quad (1)$$

$$\mathbf{H_0} = \frac{1}{\frac{R_1}{R_5}[1+\frac{C_4}{C_3}]} \quad (2)$$

$$w_0 = [\frac{1}{R_5 C_3 C_4}[[\frac{1}{R_1}+\frac{1}{R_2}]]^{1/2} \quad (3)$$

$$\mathbf{Q} = \frac{[R_5[\frac{1}{R_1}+\frac{1}{R_2}]]^{1/2}}{[\frac{C_3}{C_4}]^{1/2}+[\frac{C_4}{C_3}]^{1/2}} \quad (4)$$



S**ekil 2 a.** _kinci dereceden çok geribeslemeli süzgeç yapısı **b.** Deneyde kurulacak yapı

1.Set up the structure of figure 1b with the element given you.

2. Apply a sinusoidal input signal using the signal generator.Adjust the input signal amplitude 1V or a value smaller than 1V peak to peak. Observe and record the value of the input signal with the oscilloscope.

3.Change logarithmically the input signal frequency from 10Hz to 10MHz.Obsevre and record the output signal values for all inputs.

4.Find the lower upper cut-off frequency and center frequency.

5.Calculate the quality factor.

6.Apply square and triangular input signals at center frequency of the filter and observe the output signal. Explain the differences of the output signals between the sinusoidal,square and triangular input signals.(Don't repeat all the measurements for the square and triangular waves, only output signals will be monitored)

Note1: H_0 passing band gain , f_0 3dB frequency, Q quality factor

Note2: $Q = \frac{w_0}{w_2 - w_1}$,w_0 center frequency,w_2 and w_1 upper and lower cut-off frequency

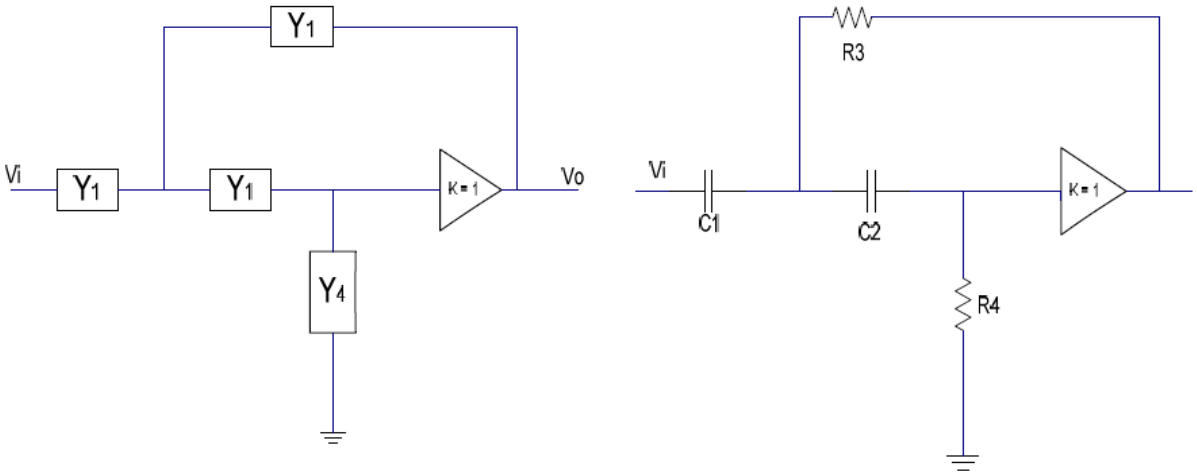
Experiment 2

$$\frac{V_o}{V_i} = \frac{Y_1 Y_2}{Y_4(Y_1+Y_2+Y_3)+Y_1 Y_2} \quad (5)$$

$$\mathbf{H_0 = 1}$$

$$w_0 = \left[\frac{1}{C_1 C_2 R_3 R_4}\right]^{1/2} \quad (6)$$

$$\mathbf{Q} = \frac{1}{\left[\frac{R_3 C_1}{R_4 C_2}\right]^{1/2} + \left[\frac{R_3 C_2}{R_4 C_1}\right]^{1/2}} \quad (7)$$



S**ekil 2 a.** _kinci dereceden birim kazançlı Sallen-Key süzgeç yapısı **b.** Deneyde kurulacak yapı

1.Set up the structure of figure 2b with the elements given you.

2. Apply a sinusoidal input signal using the signal generator.Adjust the input signal amplitude 1V or a value smaller than 1V peak to peak. Observe and record the value of the input signal with the oscilloscope.

3.Change logarithmically the input signal frequency from 10Hz to 10MHz.Obsevre and record the output signal values for all inputs.

4.Find the lower cut-off frequency.

5.Apply square and triangular input signals at center frequency of the filter and observe the output signal. Explain the differences of the output signals between the sinusoidal,square and triangular input signals.(Don't repeat all the measurements for the square and triangular waves, only output signals will be monitored)

6.Compare the solutions between the band pass filter.

EXPERIMENT 9
PLL Applications

Prelab Study

- Read through the experiment text and refered referances herein
- Review PLL applications section of CD 4046 (PLL integrated circuit) data sheets
- Review Experiment#5 notes (text, report and measurements)

Attantion

- **Prelab study** will be exemined at the begining of the lab session. You will take a **Quiz**.
- A supplementary measurement **document** will be provided in the lab.
- It is assumed that you are familiar with **foundations of PLL**. If not please review the Exp#5.
- Please remember all block diagrams except LPF are active circuits; they require decent **Power Supplies**

Aim of Experiment

The aim of this experiment for applicant is to be familiar with some applications of PLL.

Introduction

A Phase-Locked Loop (PLL) is a frequency tuning complex circuitry. It can track variation of input frequency in a range. Any information that has been encoded can be recovered by the PLL. The PLL has wide applications in industry. It is a basic building block of Telecommunication and Instrumentation systems.

Some applications are as follow

- Frequency Tuning
- FM Demodulation
- Frequency Synthesis
- Space Telemetry
- Analog Digital Converters
- Motor-Speed Control
- Instrumentation

Application#1: Frequency Tuning

Selecting a particular frequency form a composite signal has various applications. TV and Radio channel tuning are such applications. Assume several radio stations are broadcasting in an area. To receive a particular channel, the receiver should to tune to that particular radio frequency and reject the rest. To achieve the job, one can move free running frequency of VCO (PLL) to around of that particular frequency and receives the channel.

To move to another channel all one needs to do is to reposition the free running frequency around that particular channel. The free running frequency of VCO can be changed simply by a variable capacitor.

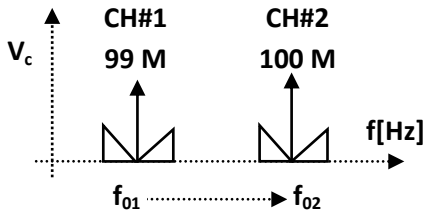


Fig. 9.1 FM Radio channel tuning example: to switch to next channel, f_0 of VCO is moved from f_{01} to f_{02} .

Measurement Circuit

To simulate frequency selection process, the following circuit will be assembled. A sine wave and a square wave are summed up to create a composite signal. Then, the PLL will be used to separate components of that composite signal. (Prescalers: LS 290, Sum circuit: uA741)

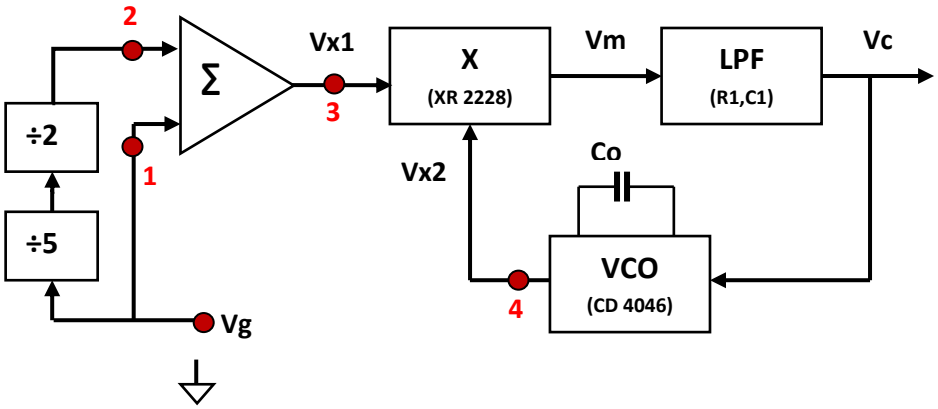


Fig. 9.2 Frequency Tuning circuit

Measurement Main Steps

(1)Use a sine wave oscillator as Vg
(2)Set sine oscillator frequency and amplitude. Typically f_1 = 10 kHz, V_{pp} = 10 V
(3)Verify node#2 frequency is (f_1 / 10)
(4)Tune capacitor of VCO to lock to sine wave
(5)Follow the steps in the supplementary sheets

Application#2: FM Modulation

An FM modulation can be realized by VCO. A VCO simply converts a voltage variation in its input to a frequency variation in its output. The linearity of (v-f) characteristic is main concern. In the following example, it is shown how a time dependent input signal (V(t)) is translated to a frequency variation (Δf) by VCO characteristic.

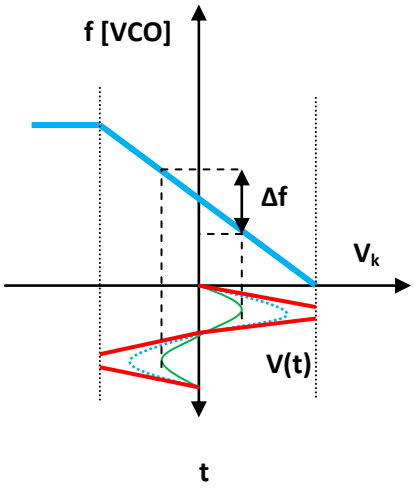


Fig. 9.3 (V-f) characteristic of VCO and applied time dependent input signals of various amplitudes

Measurement Circuit

To simulate an FM modulator the following circuit will be assembled. To get (V-f) characteristic, the input voltage will be changed in steps and output frequency will be recorded.

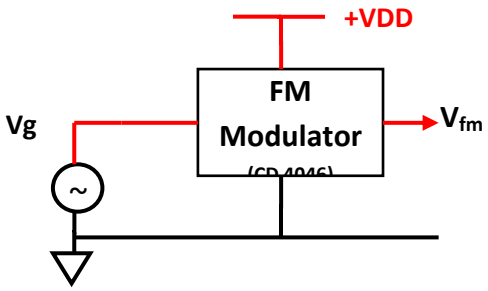


Fig. 9.4 FM Modulation circuit

Measurement Main Steps

(1)Use a sine oscillator as V_{x1} source
(2)Use an oscilloscope to display input and output signals
(3)Set sine oscillator frequency and amplitude. Typically, start with min amplitude and min frequency
(4)Follow the steps in supplementary sheets

Application#3: FM Demodulation

A PLL can be used to recover an FM modulated signal as in the case of radio receivers.

Measurement Circuit

To simulate FM Demodulation the following circuit will be assembled. First, a sine wave will be modulated with a FM modulator. Then, a PLL will be used to recover the same sine wave. If that to happen, than the mission will be accomplished.

In some applications an additional filter known as **Post Detection Filter** (PDF) is used to clarify the signal from carrier and loop`s adverse effects.

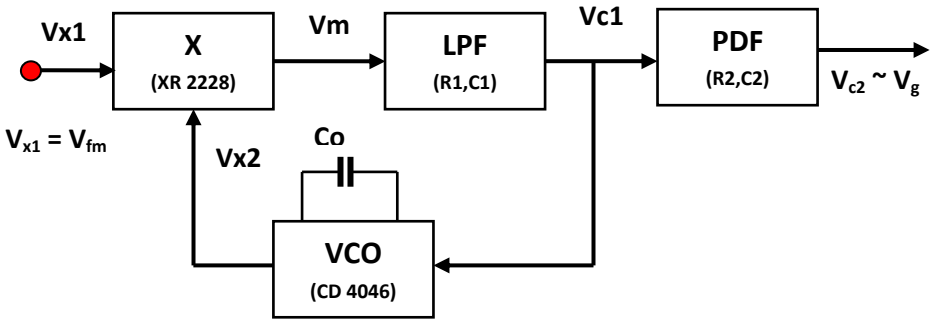


Fig. 9.5 FM Demodulation circuit

Measurement Main Steps

(1)Use a sine oscillator as V_{x1} source
(2)Use an oscilloscope to display input and output signals
(3)Set sine oscillator frequency and amplitude. Typically, f_1 = 1 kHz, V_{1pp} = 1 V
(4)Tune the VCO capacitor to recover the sine wave
(5)Follow the steps in supplementary sheets

Application#4: Frequency Synthesis

A PLL can be used to synthesize some particular frequencies. It has applications in clock delivering in integrated circuits such as microprocessors. From a very stable reference frequency such as crystal oscillators, one can derive integral and fraction of that reference signal. By PLL one can generate very precise and stable frequencies.

Measurement Circuit

To simulate frequency synthesis the following circuit will be assembled. The external input frequency will be prescaled with n-divider (÷n) and VCO will be prescaled with m-divider (÷m). For a locked PLL, both inputs of multiplier (phase detector) should have the same frequency. The following formula can be recovered from that fundamental principal.

$$\frac{f_1}{n} = \frac{f_2}{m} \tag{9.1}$$

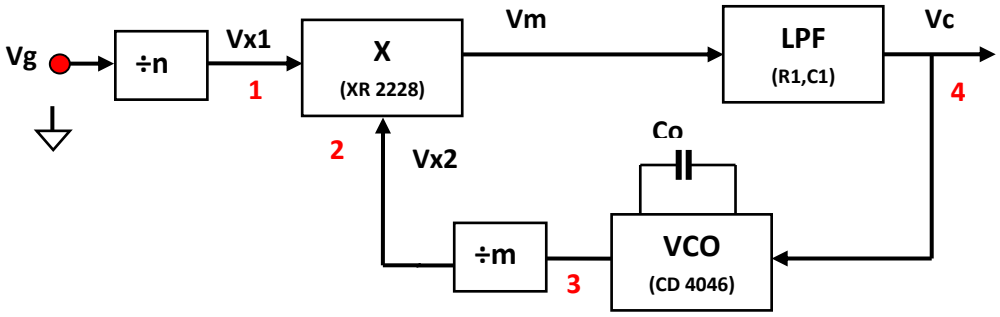


Fig. 9.6 Frequency Synthesizing circuit

Measurement Main Steps

(1)Use a TTL square wave oscillator as V_g source
(2)Use an oscilloscope to display both inputs of multiplier
(3)Set sine oscillator frequency and amplitude. Typically, f_1 = 10 kHz, V_{gpp} = ~5 V (TTL output)
(4)Tune the VCO capacitor to lock the PLL
(5)Follow the steps in supplementary sheets

References

[1] ITU "Yüksek Frekans Laboratuvarı Deneyleri", Ed.3, ITU, 1984.
[2] WILLIAMS, Arthur B., "Designer's Handbook of Integrated Circuits", McGraw-Hill, (1984).
[3] GREBENE, Alan B., "Bipolar and MOS Analog Integrated Circuit Design", (1984).
[4] BEST, Roland E., "Phase Locked Loops", McGraw-Hill, (1984).
[5] Tietz, U, and Schenk, Ch, "Electronic Circuits", Springer, 1991.
[6] www.google.com, Key words: PLL applications, FM demodulation, Frequency tuning, Frequency synthesis

[R0.2, 2/2013, AD]

EXPERIMENT 10

Switching Voltage Regulators

Preliminary work

Useful topics

- Switching power supplies
- Operating principle of LM3524 integrated circuit
- Saturation voltage values of power transistors
- Forward biasing voltage values of power diodes

Theoretical calculations

- Derive the Equation-9 including the calculations which are not written in the manual.
- Derive the Equation-13 including the calculations which are not written in the manual.
- Derive the Equation-17 including the calculations which are not written in the manual.

P.S.: "Useful topics" is not required as written. Related topics should be researched/ studied in order to understand the experiment better. Theoretical calculations and printed PSpice simulations will be collected and scored as "preliminary report". In addition, written/oral exam performed during/before the experiment, will be graded as a part of "experiment score."

Objectives:

Regulators are structures which produce voltages used for supplying electronic circuits. It is also expected that a regulator circuit should keep the voltage as constant as possible.

Knowledge:

Two kinds of regulator circuits are used commonly which are linear regulators and switching voltage regulators. Linear voltage regulators which has been investigated during Introduction to Electronics Laboratory, consists of a voltage source which has a transformer, diode and capacitor and a regulator circuit connected as series to the source. Since most part of the power is lost on the transistor of regulator circuit, the efficiency is low for these kind of circuits (%25-%50). The most important advantage of switching voltage regulators is high efficiency. In addition, the output voltage can be higher than the input signal or it can be inverted. On the other hand, switching voltage regulators have some disadvantages:

- The control circuit is more complex.
- Ripple in output voltage is higher.
- It responds more slowly to changes of load.
- It causes electromagnetic interactions and radio frequency interference.
- It is not useful for the circuits which process low-level signals.

The output signal of a switching voltage regulator is produced averaging a time-varying signal which is produced by turning on/off a transistor. Control circuit turns on/off the switch in order to adjust the output signal as desired.

A switching voltage regulator circuit consists of 3 stages:

1- A power transistor which is used for switching
2- A control circuit which is used to adjust duty cycle
3- An output circuit which converts pulsed input power into continuous output power.

We can classify switching voltage regulators in terms of output circuit:

1- Single-ended inductor circuits
2- Diode-capacitor circuits
3- Transformer coupled circuits

The first and second types of circuits can be grouped into three: Step-up, step-down and polarity inverting circuits. Circuit schemas for single-ended inductor circuits are given in Figure 10.1.

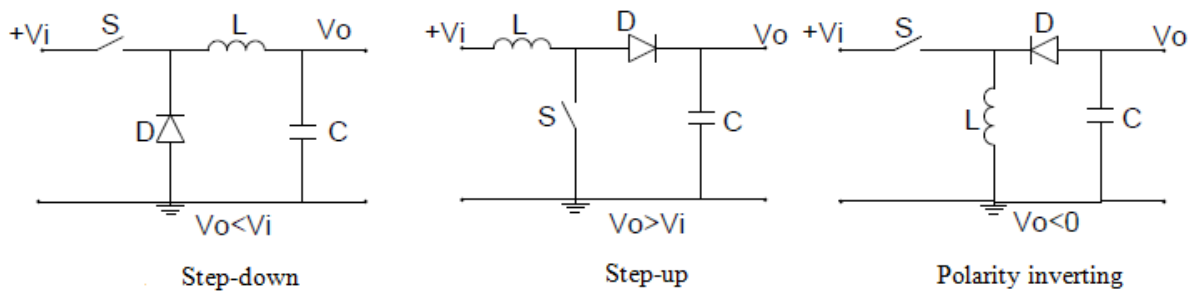


Figure 10.1 Single-ended inductor circuits

As seen in the figures, the output voltage of step-down circuit is lower than the input, the output voltage of step-up circuit is higher than the input and the output voltage of the polarity-inverting circuit is opposite in polarity to the input.

Diode-capacitor circuits are not useful to supply high-current circuits. They are generally used as voltage-multiplier. Transformer coupled circuits are used to supply high-current circuits.

On the other hand, switching voltage regulators has three types in terms of the method used to adjust duty-cycle:

1-Constant frequency / varying on-time

2-Constant on-time / varying frequency

3-Constant off-time / varying frequency

Controlling the circuit by constant frequency / varying on-time is implemented using pulse-width modulator (PWM). A pulse-width modulator is shown in Figure 10.2. Output voltage of the comparator is V_{CC} if sawtooth signal amplitude produced by oscillator is greater than V_k, otherwise it is V_{EE} (V_{EE}=0 for this circuit). Thus, pulse-width can be adjusted by changing V_k. The frequency of the output signal is equal to the frequency of oscillator.

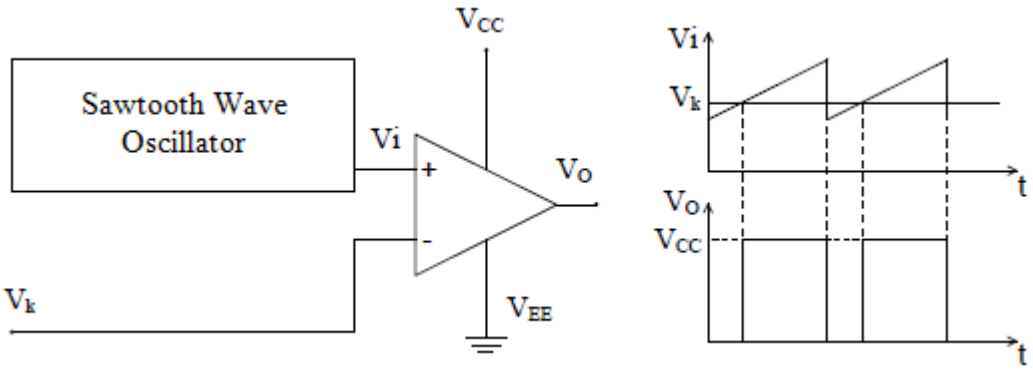


Figure 10.2 Pulse width modulator

In Figure 10.3, a switching voltage regulator in step-down mode is shown. There are lots of integrated circuits that contain parts of this block. LM3524 is one of them and it has been used in experiment board.

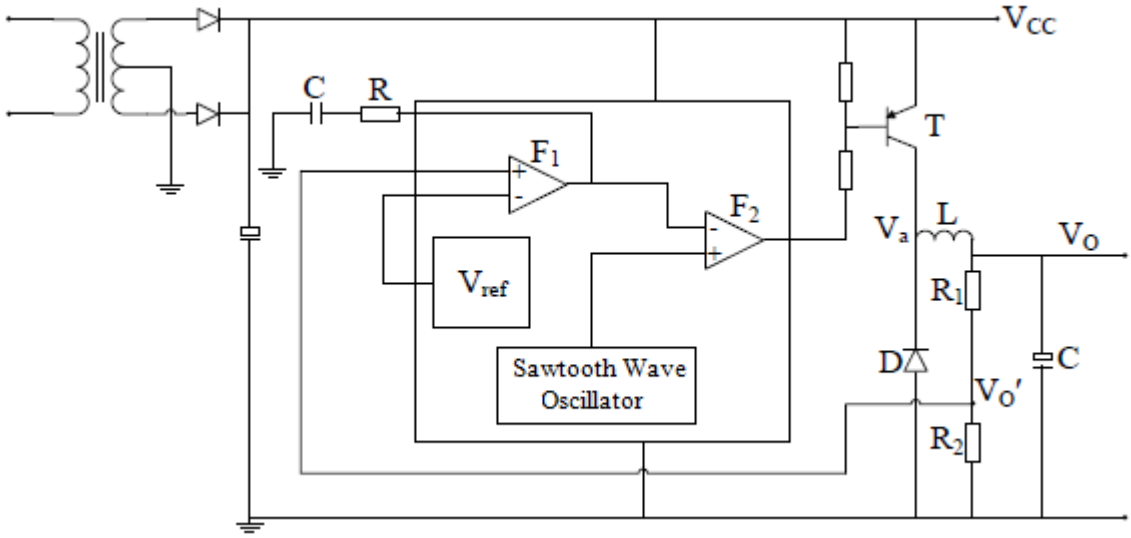


Figure 10.3 Step-down switching voltage regulator

The transistor (T) works as a switch in the circuit. When the transistor turns on, voltage on V_a node will be $V_{CC} - |V_{CEsat}|$, otherwise it will be a floating node. Average value of pulse sequence at V_a node is calculated by the output circuit which contains L,C,R components and V_o signal is obtained. Value of V_o calculated by voltage division is compared with V_{ref} by the comparator F_1. The difference is amplified and pulse width modulator is supplied. The square wave at the output of pulse width modulator is used for turning on/off the transistor. Through the negative feedback, duty cycle of the square wave at the output of PWM changes so that the difference between V_{ref} and V_o will decrease. In continuous mode, the difference approaches to zero. The output voltage is,

$$V_o = V_{ref}\left(\frac{R_1}{R_2} + 1\right) \quad (1)$$

Stability of the negative feedback is provided by R and C components. In order to operate the circuit in step-up and polarity-inverting modes, input terminals of the differential amplifier F_1 should be changed.

Step-down regulator:

The output stage of this regulator is shown in Figure 10.4. Capacitor (C) keeps the value of output voltage constant during T_{on} and T_{off} times and its value determines the ripple of output current.

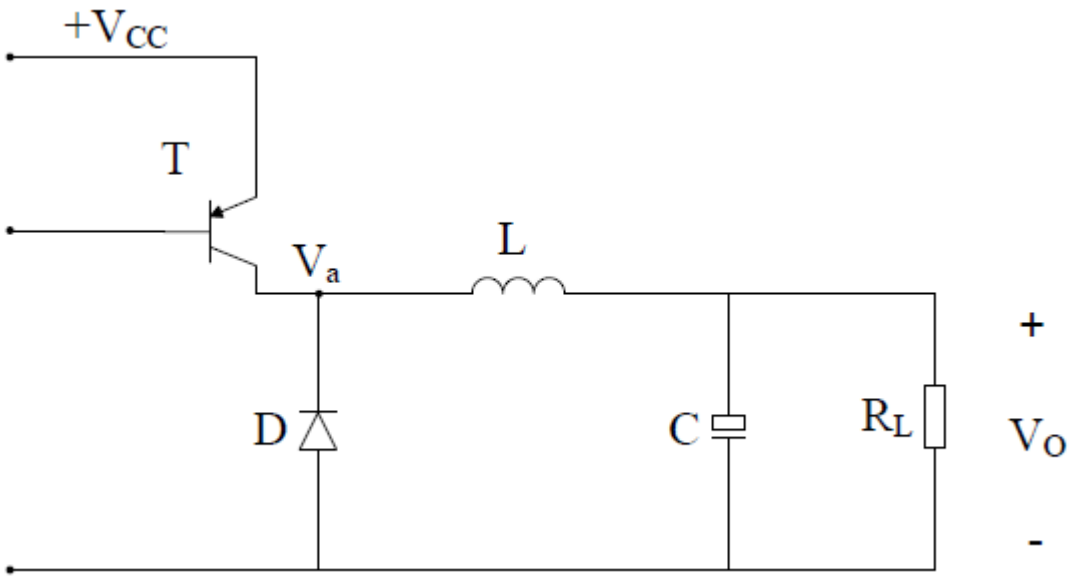


Figure 10.4 Step-Down Regulator

During T_{on} time, voltage difference across inductor is :

$$V_L = V_{CC} - |V_{CEsat}| - V_O \quad (2)$$

Voltage difference across an inductor is defined as $V_L = L.\left(\frac{\Delta I_L}{\Delta t}\right)$. If voltage difference across inductor is constant, the current increases linearly. As a result, the change of current during T_{on} is written below:

$$\Delta I_{L1} = (V_{CC} - |V_{CEsat}| - V_o).\frac{T_{on}}{L} \quad (3)$$

When the transistor turns off, the inductor changes the polarity of voltage difference keeping the polarity of current same and the diode is turned on.

During this time, the value of voltage difference across the inductor is given in Equation-4.

$$V_L = V_o + V_D \quad (4)$$

The change of current during T_{off} time is:

$$\Delta I_{L2} = (V_o + V_D).\frac{T_{off}}{L} \quad (5)$$

The change of V_a and I_L for this operation mode is shown in Figure 10.5.

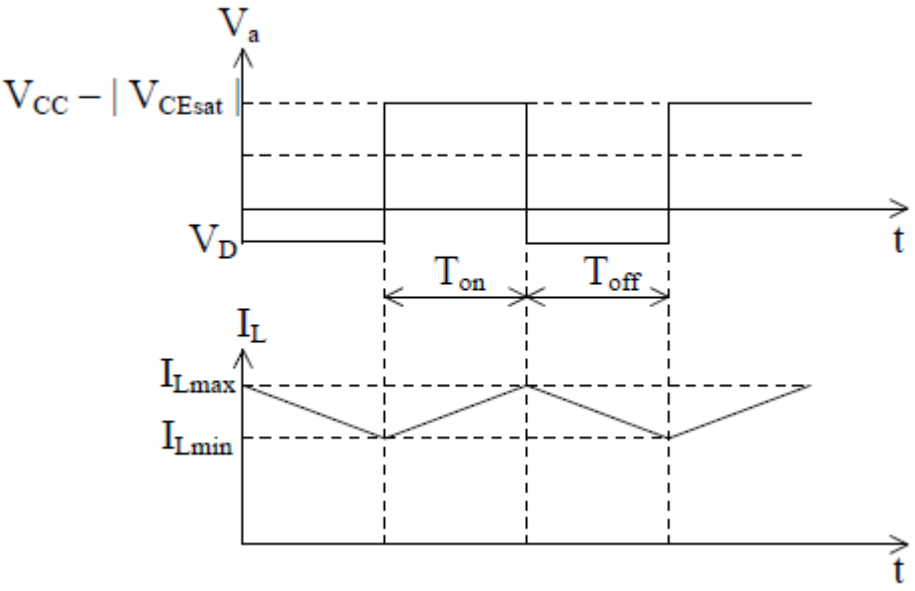


Figure 10.5 Change of $V_L$and I_L for step-down regülatör

In continuous mode, $\Delta I_{L1} = \Delta I_{L2}$ so Equation-6 can be derived.

$$\frac{T_{on}}{T_{off}} = \frac{V_o + V_D}{V_{CC} - |V_{CEsat}| - V_o} \tag{6}$$

If V_{CEsat} and V_D are ignored, the output signal can be written as in Equation-7.

$$V_o = V_{CC}.T_{on}/T \tag{7}$$

As seen in Equation-7, output voltage can be adjusted by changing T_{on}. But, output current should be higher than I_{ymin} value so that Equation-7 is valid. If a load is connected to the output and a current lower than I_{ymin} is flowed, the current which is stored by inductor during T_{on} reaches zero before T_{off} is over. As a result, the voltage difference across inductor becomes zero. Change in $V_a$and I_L for this situation is shown in Figure 10.6.

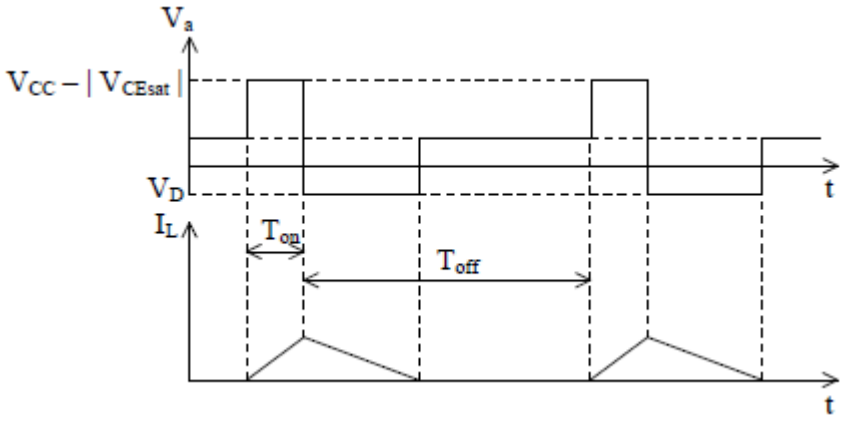


Figure 10.6 Change of Vah and IL when Io<Imin

In general, the efficiency of a power supply is given in Equation-8.

$$\eta = \frac{P_{yük}}{P_{in}} = \frac{I_o V_o}{I_{in} V_{in}} \tag{8}$$

If this equation is re-arranged using $V_{in} = V_{CC}$ and $I_{in} = I_o.T_{on}/T$, Equation- 9 is derived:

$$\eta = \frac{V_{CC}+V_D-|V_{CEsat}|}{V_D+V_o} \cdot \frac{V_o}{V_{CC}} \quad (9)$$

Step-Up Regulator:

The output stage of this regulatör is shown in Figure 10.7. Change of I_L, I_D and V_a can be seen in Figure 10.8.

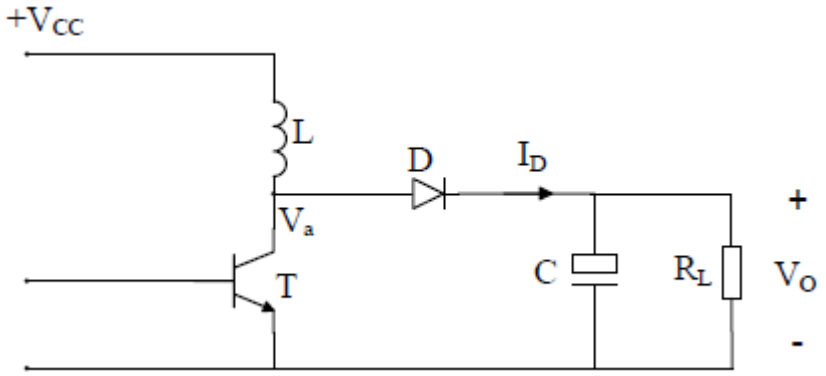


Figure 10.7 Step-Up Regulator

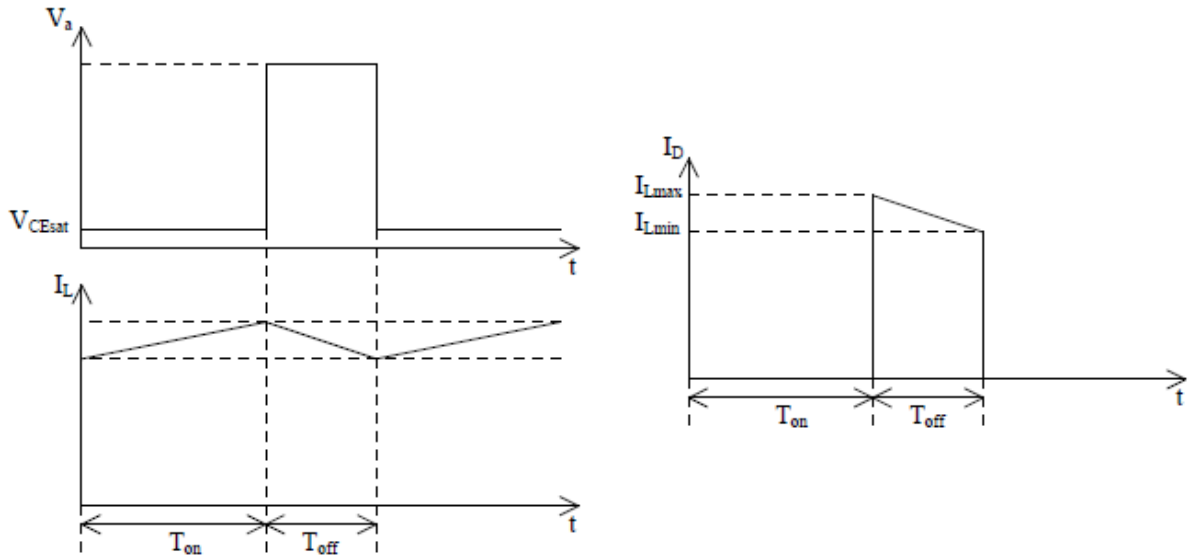


Figure 10.8 Change of V_a, I_L and I_D for step-up regülatör

The minimum value of output voltage is $V_L = V_{CC} - V_D$. The capacitor C works as the same in step-down regulator circuit.

During T_{on} time, the voltage difference across inductor is $V_{CC} - V_{CEsat}$. When the transistor turns off, inductor continues flowing the current turning the diode on. The voltage difference across inductor is $V_L = V_o + V_D - V_{ce}$. Since the change of current is equal during T_{on} and T_{off} times, Equation-10 can be derived:

$$\frac{T_{on}(V_{CC}-V_{CEsat})}{L} = \frac{T_{off}(V_o+V_D-V_{CC})}{L} \quad (10)$$

Ignoring V_D and V_{CEsat}, we can get eq.11.

$$V_o = V_{CC}\frac{T_{on}+T_{off}}{T_{off}} \quad (11)$$

The time T=T_{on} +T_{off} in the equation is the period of the signal and since it is constant if T_{off} is decreased, the output voltage gets values higher than V_{CC}. The output current should be higher than I_{min} so that these equations are valid.

The input current of step-up regulator is always higher than the output current. In the absence of signal-loss, the input and output powers are equal and $I_{in}.V_{in} = I_o.V_o$ is valid. If Equation-11 is substituted, Equation-12 is derived.

$$I_{in} = I_o.T/T_{off} \quad (12)$$

Here, I_{in}, V_{in}, I_o and V_o are the mean values. The efficiency of the circuit can be calculated using Equation-13.

$$\eta = \frac{V_{CC}-V_{CEsat}}{V_o+V_D-V_{CEsat}} \cdot \frac{V_o}{V_{CC}} \quad (13)$$

Polarity-Inverting Regulator:

The output stage and change of V_a for this regulator circuit are shown in Figure 10.9.

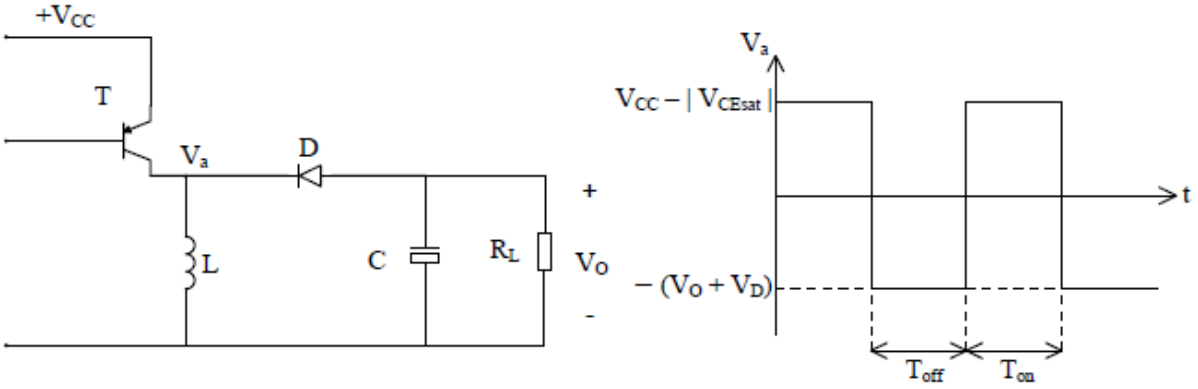


Figure 10.9 Polarity-Inverting Regulator and change in V_a

During T_{on} time of transistor, the voltage difference across the inductor is V_L-V_{CC}-|V_{CEsat}|. When the transistor turns off, the inductor changes the polarity of voltage difference across it, keeping the polarity of current same. It continues flowing the current turning the diode on**.** During this time, V_L=-(V_o+V_D).

In continuous mode, the change of current during T_{on} and T_{off} are equal so, Equation-14 can be written as:

$$\frac{T_{on}(V_{CC}-|V_{CEsat}|)}{L} = \frac{-T_{off}(V_o+V_D)}{L} \quad (14)$$

Ignoring V_{CEsat} and V_D, Equation- 15 can be derived.

$$V_o = -V_{CC}\frac{T_{on}}{T_{off}} \tag{15}$$

Equation- 15 is valid if the output current is higher than I_{min}. For the current values lower than I_{min}, the situation written in step-down regulator occurs.

The input current of regulator is written in Equation-16 and efficiency can be calculated using Equation-17.

$$I_{in} = |I_o|.{}^{T_{on}}\!/_{T_{off}} \tag{16}$$

$$\eta = \frac{|V_o|}{V_D+|V_o|}\cdot\frac{V_{CC}-|V_{CEsat}|}{V_{CC}} \tag{17}$$

References

1. H. H. Kuntman, Endüstriyel Elektronik, Birsen Yayınevi, İstanbul, 2003
2. M. S. Türköz, Elektronik, Birsen Yayınevi, İstanbul, 2004.
3. D. Leblebici, Elektronik Devreleri, İTÜ Matbaası, 1992.

Analog Electronic Circuits Laboratory

Procedure Sheet

Experiment #10 – Switching Voltage Regulators

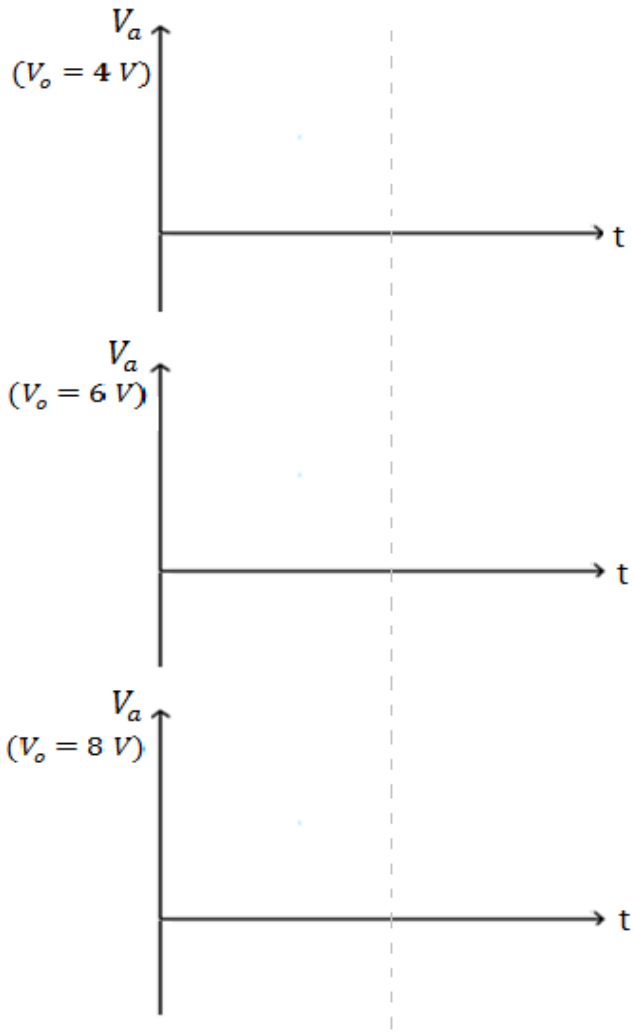
Date		**Group**	**Student ID**	**Student Name**
Assistant				
Signature				

Procedure:

1. Construct the circuit given in Figure 10.4. Set the switch to Step-Down. Connect the oscilloscope to the V_a node in order to observe the signal.

a. Adjust the output voltage to 4V,6V and 8V respectively, using tunable resistor on the board. For each of these conditions, adjust the load so that the output current will be higher and lower than I_{min}, respectively. Sketch V_a signal. (Load current shouldn't be higher than 400 mA).

$I_o > I_{min}$ $I_o < I_{min}$

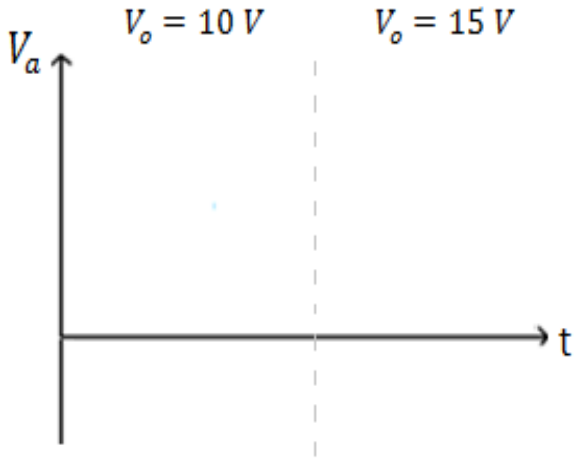


b. Adjust the load so that output voltage is 4 V and output current is 100 mA. Then, change the output voltage without changing the load and fill in the table below.

V_o	4 V	5 V	6 V	7 V	8 V
V_{in}					
I_o					
I_{in}					

2. Construct the circuit given in Figure 10.7. Set the switch to Step-Up.

a. Set the output voltage to 10 V and adjust the load so that output current is 80 mA. Observe the V_a signal on oscilloscope and sketch it. Then, set the output signal to 15 V and sketch the V_a signal again.

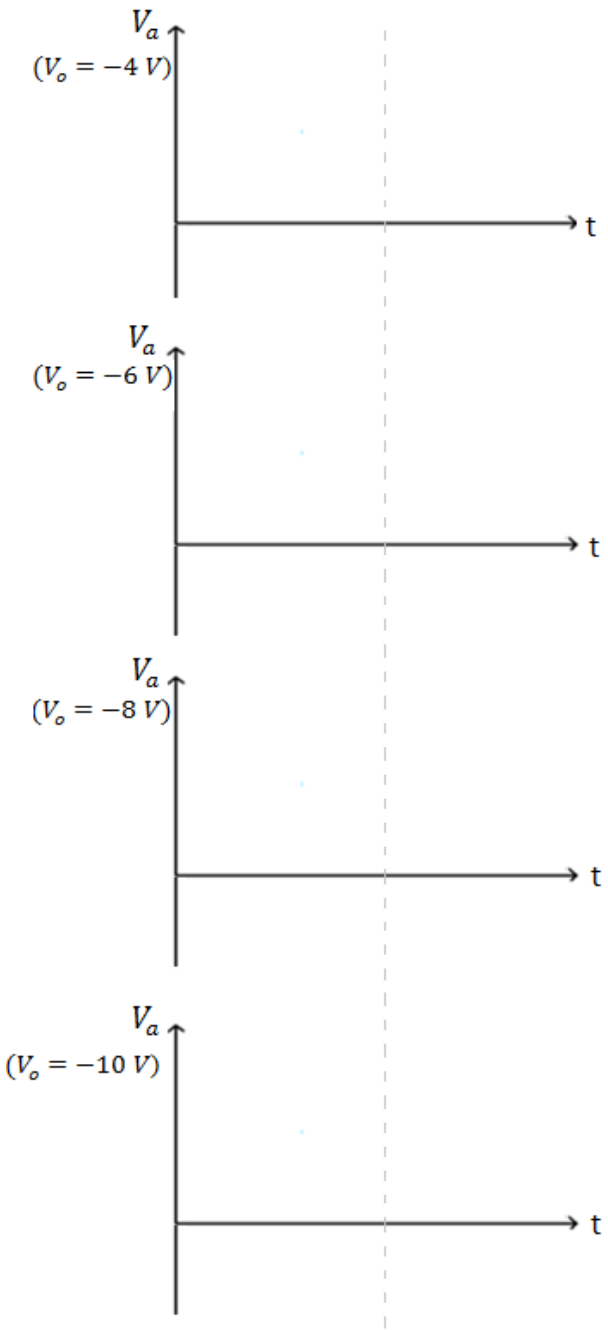


b. Change the output voltage and measure the output current, input current and input voltage.

V_o	10 V	12 V	14 V	16 V
V_{in}				
I_o				
I_{in}				

3. Construct the circuit given in Figure-10. Set the switch to polarity-inverting.

a. Adjust the output voltage to -4V, -6V, -8V and -10V respectively. Sketch the V_a signal for each situation so that output current is higher than I_{min} . (Load current shouldn't be higher than 400 mA)



b. Set the output voltage to -2 V and adjust the load so that output current is 80 mA. Then, change the value of output voltage from -2V to -10 V, and measure the input voltage and current. (For each value of output voltage, load should be adjusted again, to set the output current to 80mA.)

V_o	-2V	-4V	-6V	-8V	-10V
V_{in}					
I_{in}					

Requirements for the report :

1) Compare the signals you plotted with the ones in laboratory manual. If they are different, explain the reason.

2) Using the values you measured during the experiment, plot the graph of output voltage versus efficiency of each circuit.

3) Choose one of the circuits used for the experiment and make simulation using PSpice. Use the circuit in Figure-3 for switching and supply the circuit usin 10V DC source. You should use power diode and power transistor. Compare your simulation results with the ones you measured. Comment on the results.