1. Experiment Purpose & Foreknowledge

With the rapid improvement of integrated circuits technology in the electronics field, the integrated circuits have been replaced the discrete circuits elements. The integration of the circuits has a lot of benefits and it is responsible for the rapid grow in the electronics industry. Some of these advantages are fabrication of identical circuits, small size with high performance and reliability. The first half of the 80s, bipolar and MOS technologies are used in analog and digital circuit designs. After 90s, MOS technology has been widely used and it dominated the analog circuit designs as well. Recently, CMOS is the primary process in both digital and analog/RF/mixed-signal circuits.

The current sources are the main circuit elements which are used for either biasing circuits or as an active loads for amplifiers. Generally, in an IC chip with a number of amplifier stages, a constant, reliable DC current (called as reference current) is generated in one circuit block, and it is replicated to use at different locations in the chip for biasing the different amplifier stages. The basic idea is to use a reliable, special circuit to generate this predictable and stable current so that replicas of that current also has the same characteristics. Otherwise, the biasing currents generated at different locations would be significantly different which degrades the circuit performance or even causes the malfunction. In this way, if the current reference does not change with process, voltage and temperature variations, then replicas do not change, too. Apart from bias operation, a current source can be also used as an active load for amplifiers. Unlike a resistor, transistors in forward-active (BJT) or saturation (MOSFET) region has high output resistance across a wide voltage range. This property makes them beneficial to obtain high gain from amplifiers.

2. Experiment Setup

In Fig. 1, a basic MOS current mirror is shown. Q1 is in diode connected configuration (V_G is connected

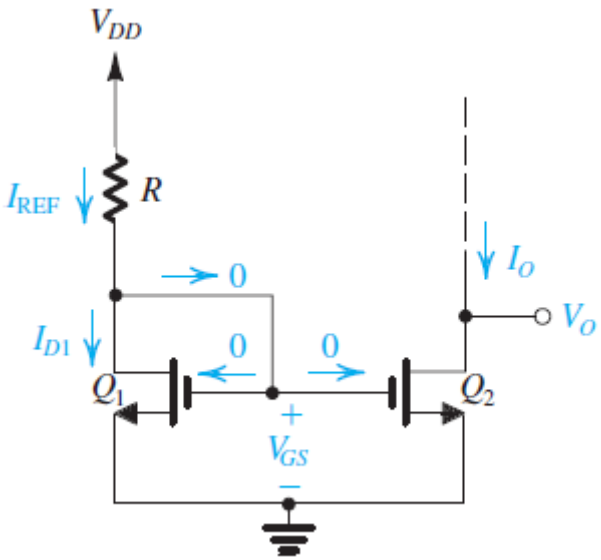


Fig. 1: A basic MOS current mirror.

to the V_D) which ensures the saturation region operation. From the circuit:

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

From the figure, it is obvious that V_{GS} voltages are the same for both Q1 and Q2. If we assume that Q2 is operation in the saturation region and ignore the channel length modulation, then:

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

The equation shows that the reference current can be replicated and scaled by the aspect ratios of the transistors. The term "current mirror" is originated from this property. The important condition to keep in mind is that, transistors must be in saturation. Fig. 2 shows the current change due to the operation region and channel length modulation.

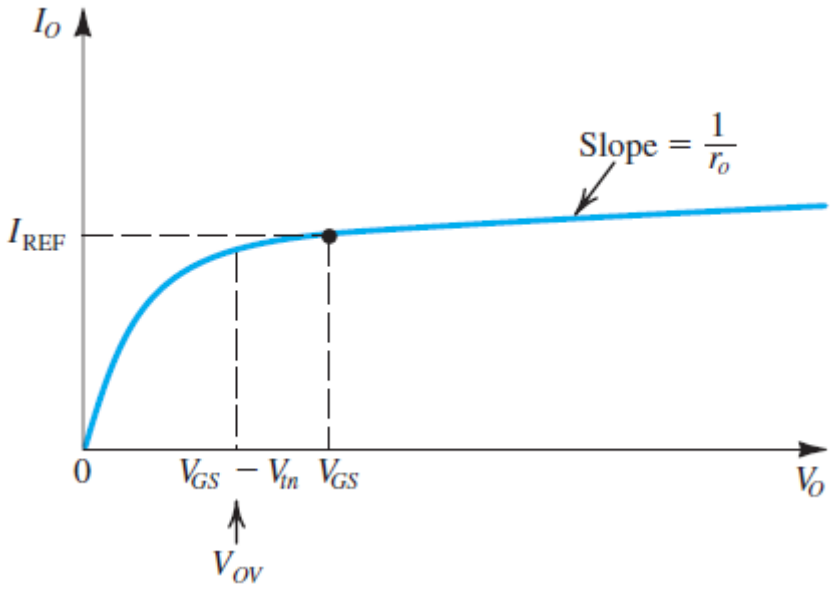


Fig. 2: Output characteristics when Q2 is matched with Q1.

From the figure we can conclude that, to obtain exactly the same current (or scaled version of it if aspect ratios are different) from the reference, Q1 and Q2 must have the same V_{DS} voltages, which is the V_{GS} voltage of Q1 since it is diode-connected. The channel length modulation causes change in current depending on the output resistance of the MOSFET. The equation can be given by:

$$I_O = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left(1 + \frac{V_O - V_{GS}}{V_{A2}}\right)$$

where V_A is the channel length modulation parameter.

Finally, the complete current distribution scheme can be found in Fig. 3. Here, you can see the PMOS current mirrors. Sometimes NMOS current mirror is called as current sink (because it sinks the current) whereas PMOS current mirror is called as current source (because it sources the current). Also, another name for the circuit in Fig. 3 is the current-steering circuit.

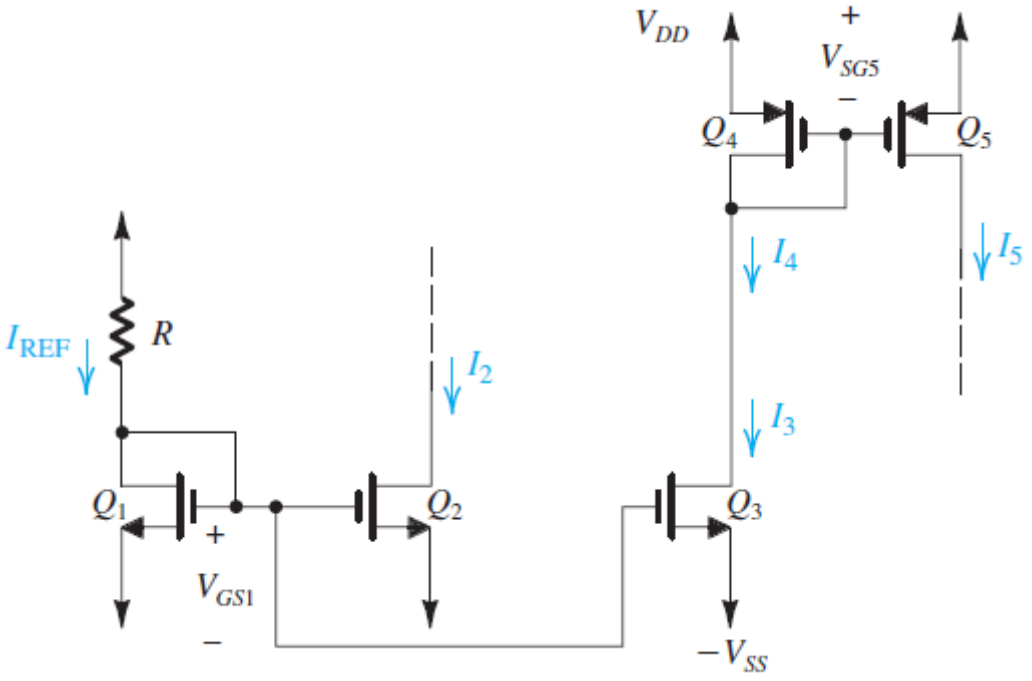
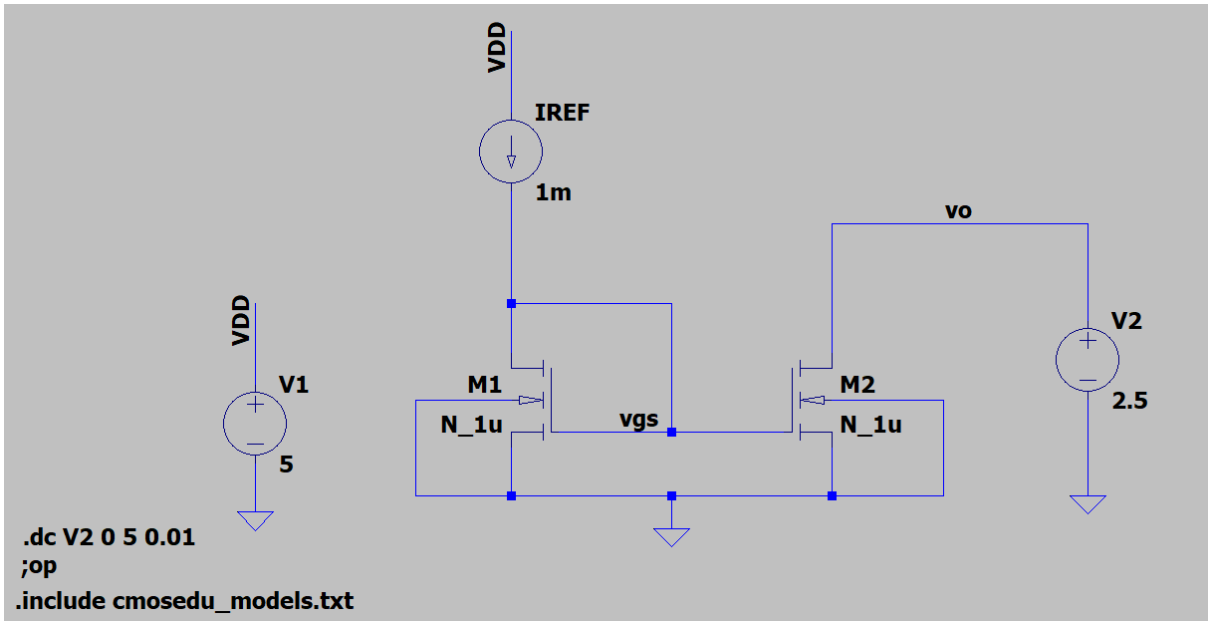


Fig. 3: A current-steering circuit.

3. Experiment Procedure

In this experiment, you need to use long channel (1µm) CMOS models given at the end of this document. You can also download the model file from R. Jacob Baker - CMOS Circuit Design, Layout, and Simulation. Always use 1µm channel length through the experiment.

Experiment 1:



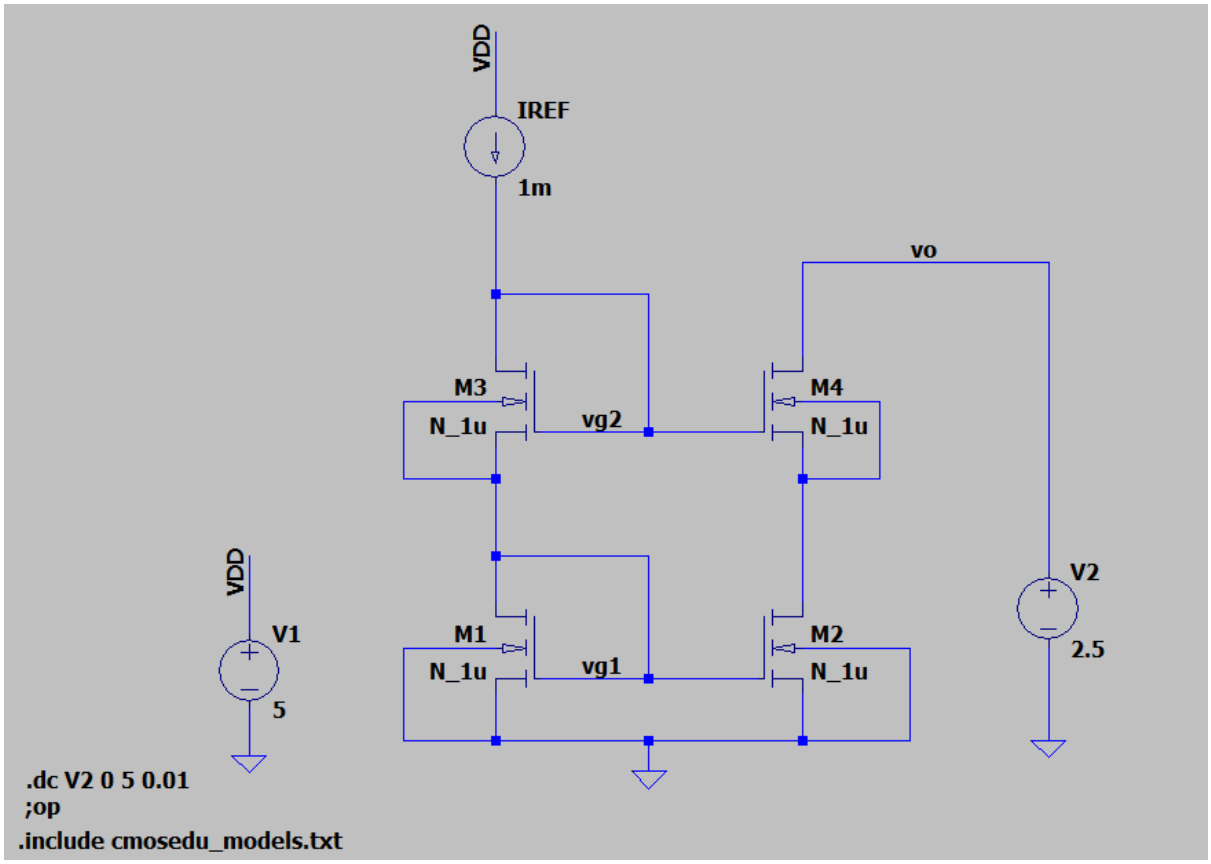
Set up the circuit above in LT Spice. VDD = 5V, IREF = 1mA, W = 100u for both M1 and M2. Set the voltage of V2 as VDD/2 which is 2.5V

a) First run a DC op. simulation and note vgs node voltage value. Then, go View→ Spice Error Log and note Vdsat value for both M1 and M2 which is V_{GS}-V_{TH}.

b) Run a DC sweep simulation for V2 (equivalently vo). Use linear sweep, Start Value: 0, Stop Value: 5, Increment: 0.01. Plot I_D of M2. Find and note the approximate point where M2 enters the saturation region. Find and note where the current is equal to the IREF. Finally, using 2 cursors, select 2 point on the plot where M2 is in the saturation region and calculate Rout = ΔV/ΔI.

c) Change the W = 200u only for M2 and repeat a) and b) for this value. Remember, this time the current of the M2 will be twice of the IREF.

Experiment 2:

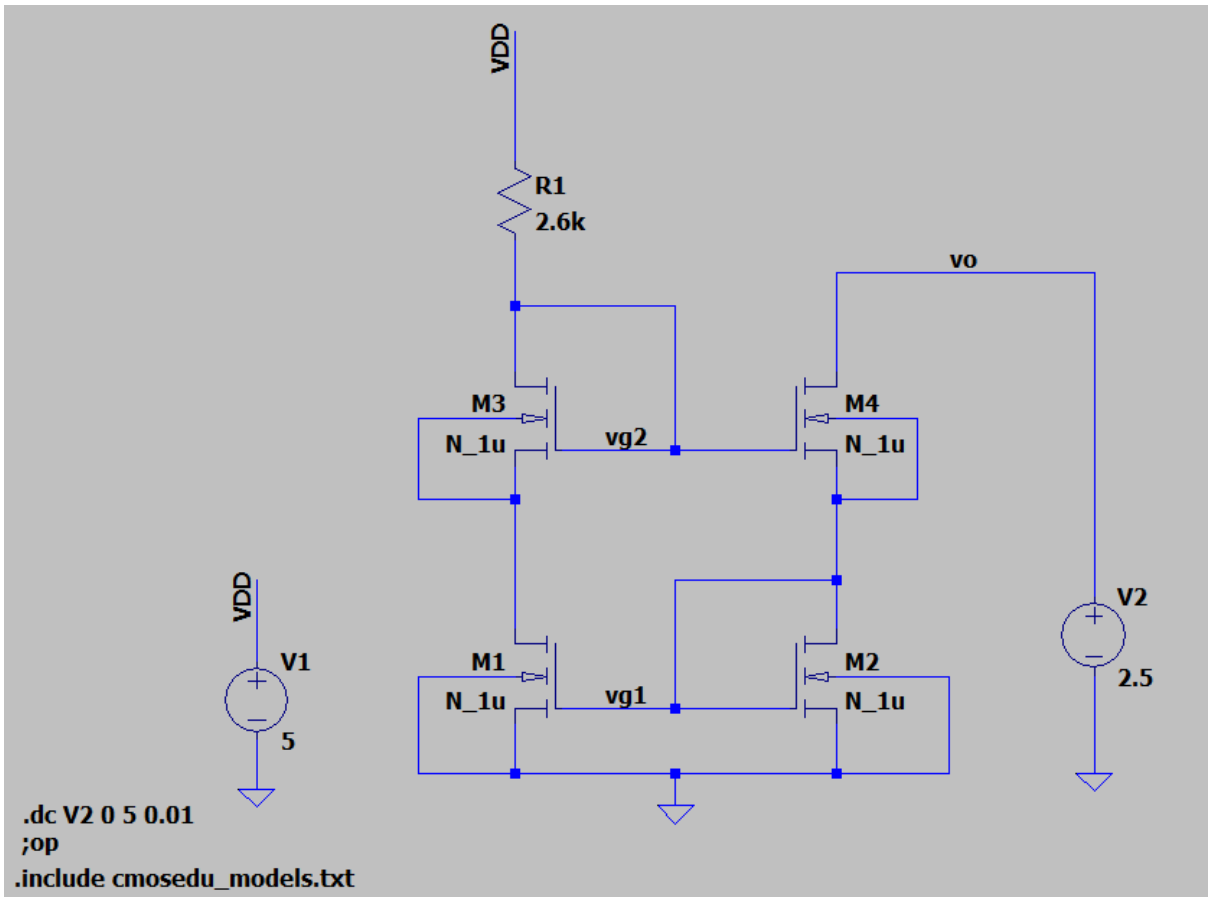


This figure shows a cascode current mirror. All of the MOSFETs are identical and W = 100u.

a) Repeat the same procedure from the 1st experiment. This time note vg1, vg2 and Vdsat values.

b) Run DC sweep simulation using the same parameters before. Plot I_D of M4 and repeat the steps in the 1st experiment part b). You do not need to repeat part c).

Experiment 3:



This figure shows the Wilson current mirror which is the slightly modified version of the cascode mirror. For this setup, include a 2.6kΩ resistor as shown in the figure to get IREF. All MOSFETs are identical with W = 100u. For this setup, only run DC sweep simulation and plot both I_{D3} and I_{D4} for M3 and M4. Observe that, unlike the previous cases (IREF was always the same for the left branch independent of the vo voltage), two branches are dependent to each other. This is the main reason why we cannot use ideal current source for this circuit. V_{GS} voltage of the M1 is set by M2, if M2 is in cut-off, M1 must be in cut-off as well. If we use ideal current source, this condition is impossible. For this circuit, only calculates the Rout using cursors as explained before.

4. Experiment Report

In the report, please include the analytical expressions for each circuit. (Hint: You might want to review Sedra & Smith's book) Please derive the conditions for V_O where circuit works as a current source. Also find analytical expressions of Rout (which is the small-signal resistance looking into the V_O node) and compare them. Based on the theoretical analysis, justify your simulation results using the operation point values from the a) parts. Discuss the advantages and disadvantages (in other words, trade-offs) of each circuit topology.

References:

-Sedra, A. S & Smith, K. C. (2009). *Microelectronic circuits (6th Edition)*. Oxford University Press.

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Model Parameters:

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* Long channel models from CMOS Circuit Design, Layout, and Simulation,
* Level=3 models VDD=5V, see CMOSedu.com
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.MODEL N_1u NMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.5
+ PHI    = 0.7           VTO    = 0.8          DELTA  = 3.0
+ UO     = 650           ETA    = 3.0E-6       THETA  = 0.1
+ KP     = 120E-6        VMAX   = 1E5          KAPPA  = 0.3
+ RSH    = 0             NFS    = 1E12         TPG    = 1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
*
.MODEL P_1u PMOS LEVEL  = 3
+ TOX    = 200E-10       NSUB   = 1E17         GAMMA  = 0.6
+ PHI    = 0.7           VTO    = -0.9         DELTA  = 0.1
+ UO     = 250           ETA    = 0            THETA  = 0.1
+ KP     = 40E-6         VMAX   = 5E4          KAPPA  = 1
+ RSH    = 0             NFS    = 1E12         TPG    = -1
+ XJ     = 500E-9        LD     = 100E-9
+ CGDO   = 200E-12       CGSO   = 200E-12      CGBO   = 1E-10
+ CJ     = 400E-6        PB     = 1            MJ     = 0.5
+ CJSW   = 300E-12       MJSW   = 0.5
*
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